Quadruple GEM PCB simulator *

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A major upgrade of the ALICE TPC is foreseen during the LHC Long Shutdown 2 (2019-20) when the existing MWPC-based readout chambers will be replaced with detectors employing the Gas Electron Multiplier (GEM) technology. The key parameter for a long-term operation of the GEM-based TPC is the stability against electrical discharges. A thorough investigation of the discharge properties of GEM-based detectors has been already reported by the Collaboration in e.g. [1].

The next important goal is the final assessment of the HV supply scheme planned to be used with the upgraded readout chambers. Behaviour of the system in case of a spark occurrence, propagated discharges or an emergency trip of a power supply is of a great importance. A possibility of the overvolatge across any GEM foil must be avoided by any means. In order to test the reaction of the powering scheme on the violent events, as listed above, we have designed and built a GEM detector simulator based on the conventional electronic elements.

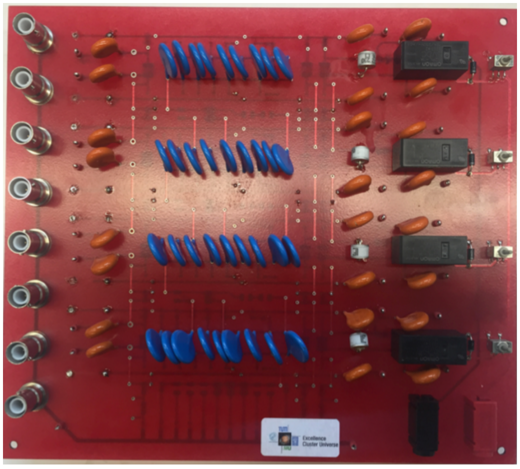

Figure 1: Quadruple GEM PCB simulator

Figure 1 shows a picture of a double-layer PCB (top view) equipped with capacitors and resistors corresponding to the realistic values of a quadruple GEM Inner Read-Out Chamber for the upgraded ALICE TPC. HV is applied to 8 channels (corresponding to 8 GEM electrodes) via SHV connectors. The device allows for a simulation of a short in one of GEM segments (in each layer) using HV relays or a spark occurrence by employing a Gas Discharge Tube (GDT) which creates a spark after a breakdown voltage is reached. GDTs can simulate a discharge across one segment of GEM (its equivalent capacitor) or between GEMs in one of the transfer or induction gaps and their breakdown voltage corresponds to the realistic settings applied to the detectors. Voltages on electrodes in question can be monitored on a scope using standard 1:10 probes via decoupling HV capacitors, included in the design.

An example of operation of the PCB simulator is presented on figure 2, where a GEM discharge signal recorded with a real detector (top panel) is compared to the one recorded with the GEM PCB simulator (bottom panel, scope screenshot). The signal waveform shows modulations which are due to the inductance of the system, resulting in periodic oscillations. The signal form the simulator nicely reproduces main features of the real signal, such as amplitude, length, oscillation period.

The device presented in this report can serve as a testing tool for the assessment of the HV scheme without a need to use a real detector.

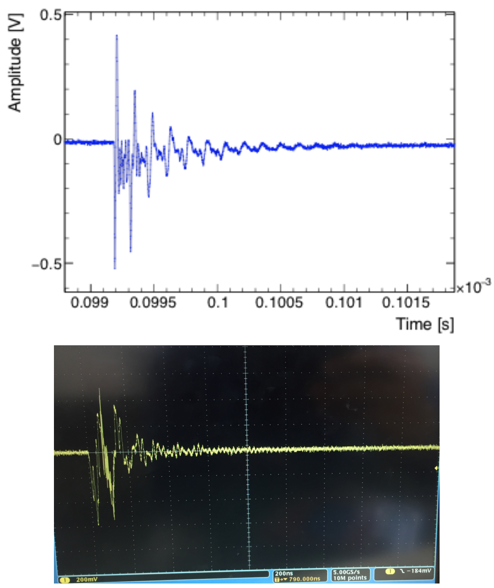

Figure 2: Discharge signal recorded with a real detector (top) and with the GEM PCB simulator (bottom).

References

[1] ALICE Collaboration, CERN-LHCC-2015-002 (ALICE-TDR-016-ADD-1) 2015

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