Technische Universität München

Development of a GHz Sampling ADC for the CALIFA Calorimeter

Masterthesis
by

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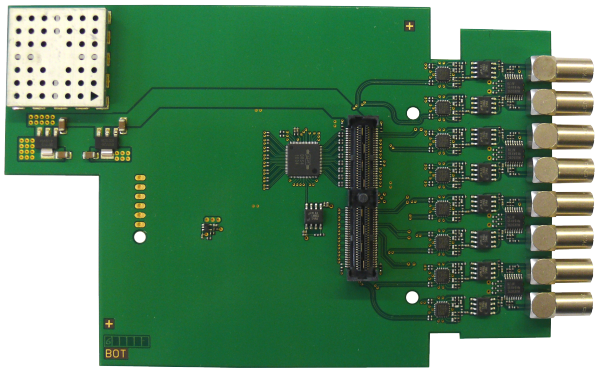

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Abstract

The new Facility for Antiproton and Ion Research (FAIR), which is currently under construction at the GSI Helmholtz Center in Darmstadt, will provide high intensity primary and secondary beams enabling studies of exotic nuclei far beyond stability. The Reactions with Relativistic Radioactive Beams (R3B) setup is one of the new experiments at FAIR, with the electromagnetic calorimeter CALIFA surrounding the target for kinematically complete reaction studies. The CALIFA Endcap Phoswich Array (CEPA) in the most forward direction of the detector uses the fast scintillator materials $LaBr_3$(Ce) and $LaCl_3$(Ce) for the detection of γ-rays and light charged particles with energies up to 700 AGeV.
To allow a homogeneous fully digital readout of the whole calorimeter, an add-on electronics board for GHz sampling of the CEPA was developed in the framework of this thesis. A basic concept based on a switched capacitor array for buffering of the analog signals and a parallel integrator circuit for readout trigger generation was worked out. The first prototype of the add-on board processes eight analog input channels and samples the high frequency signals with one Domino Ring Sampler 4 (DRS4) at 1 GHz. For each channel three different gain stages were implemented to allow a selection of the input range of interest. The prototype was tested with exemplary exponentially decaying signals and showed a good analog preprocessing with consistent decay times at the DRS4 inputs. An very good energy resolution of 0.14% (FWHM) was achieved for the integrator branch.
In the outlook the ongoing work on revision 2 of the addon-board and discussed changes to the readout structure are described.

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Chapter 1

Introduction

1.1 FAIR and R^{3}B

The study of fundamental processes of strong and electroweak interaction utilizes more and more high-energetic, exotic particle beams far beyond the "valley of stability". This will be a major pillar of the ***F**acility for **A**ntiproton and **I**on **R**esearch* (**FAIR**, see figure 1.1), which is currently under construction at the *GSI Helmholtz Center for Heavy Ion Research* in Darmstadt. The present linear accelerator *UNILAC* and the ring synchrotron *SIS18* are

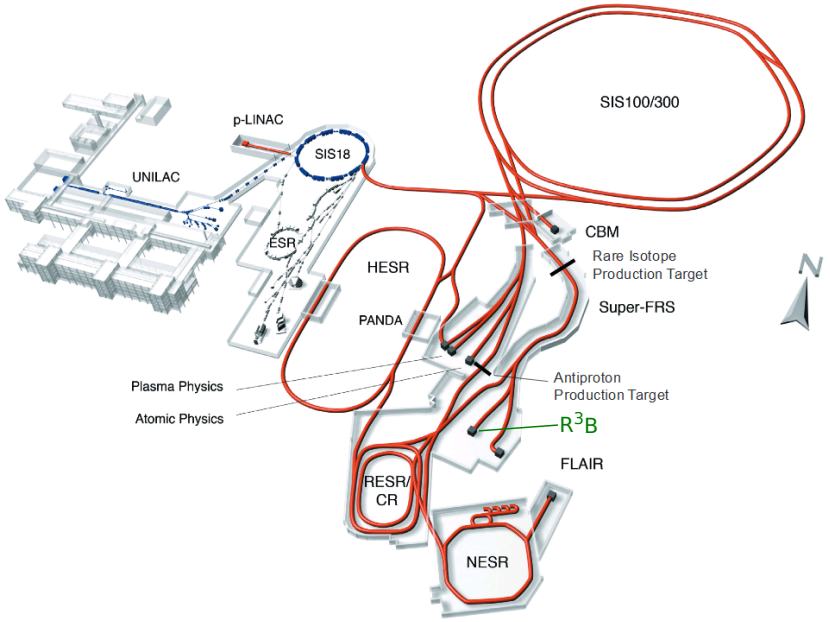


Figure 1.1: Currently constructed FAIR facility (red) at the GSI in Darmstadt. The existing facilities (blue) will be used as preaccelerators for the double synchrotron *SIS100/300*. The R^{3}B experiment (green) is positioned in the high energy branch of the Super-FRS Spectrometer. This picture was adopted from [1].

used together as preaccelerators for the new Dual Ring Synchrotron *SIS100/300*, which will provide primary beams with energies of up to 34 AGeV (U^{92+}) [1]. The superconducting fragment separator *Super-FRS* will be the main instrument to provide short-lived exotic secondary beams in a wide energy range and with high purity and intensity up to energies larger than 1 AGeV [2]. In the high-energy branch of the *Super-FRS* sits the ***R**eactions with **R**adioactive **R**elativistic **B**eams* (**R^{3}B**) setup for fixed target experiments. This magnetic spectrometer

will allow for kinematically complete measurements in inverse kinematics. The challenge for a setup like this is the ability to detect and accurately characterize each particle emitted from the target reaction. The different components of the R^3B spectrometer are shown schematically in figure 1.2. The beam-particle's momentum and specific energy loss are characterized

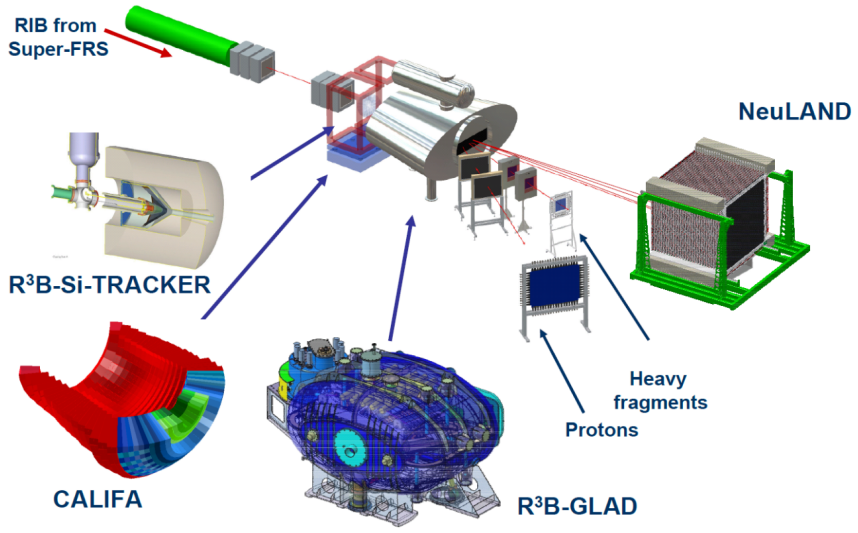


Figure 1.2: Scheme of the R^3B spectrometer setup. Picture taken from [3].

by position-sensitive silicon panel trackers, before they hit a secondary target. Target-like reaction products are detected by the surrounding silicon tracker and the *CALIFA* calorimeter. In forward direction emitted projectile-like particles enter the superconducting dipolmagnet *GLAD*. They are deflected according to their mass-to-charge ratio and measured by high-resolution detectors subsequently. The highly efficient neutron detector *NeuLAND* can be placed in a distance of 10 m up to 35 m from the target. Another spectrometer branch for high resolution measurements will be realised in the second stage of the project [4].
This setup allows the detailed study of the structure of exotic nuclei by reactions like [5]:

- **Knockout reactions and quasi-free scattering**: A common way to study the single particle structure of exotic nuclei is to use knockout reactions, which add or remove single nucleons, especially in the halo of light exotic nuclei. The new facility provides brilliant heavy neutron-rich nuclei in sufficient intensity allowing nuclear structure studies very far from stability. With beam energies of up to 700 AMeV the nucleus becomes nearly transparent for the reaction products, enabling the study of deeply bound nucleons by a quasi-free scattering as well.

- **Electromagnetic excitation**: Proton-rich heavy ions with energies far above the Coulomb barrier interact in peripheral collisions also via the electromagnetic force. The use of energies of about 1 AGeV allows to study the excitation energies of collective nuclear states.

- **Spallation reactions**: To reconstruct the excited state before a spallation, all products have to be identified in mass and nuclear charge. With R^3B the competition between different de-excitation mechanisms can be studied also for heavy projectiles.

1.2 CALIFA

The ***CAL****orimeter for* ***I****n-****F****light detection of* γ*-rays and high energy charged p****A****rticles* (depicted in figure 1.3) is of special importance for the kinematically complete measurements with R^3B. Surrounding the secondary target, it covers nearly the full solid angle of 4π in the center-of-momentum frame. Due to the fixed-target character of R^3B most particles are

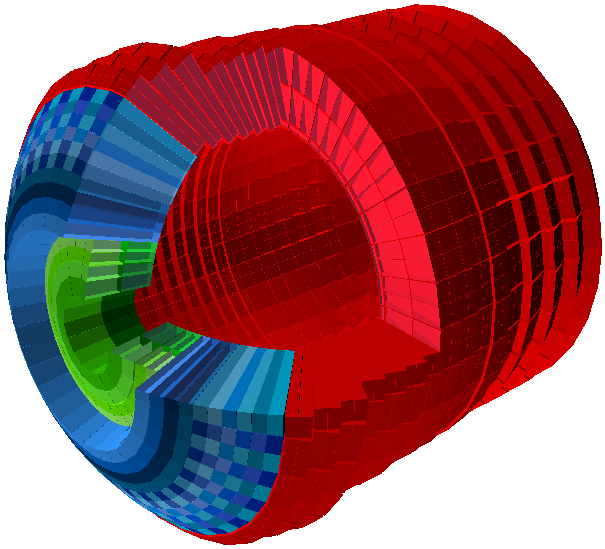


Figure 1.3: Technical drawing of *CALIFA* with the *Barrel* in red, the *iPhos* part in blue and *CEPA* in green.

emitted in forward direction with a considerable Lorentz-boost. The resulting requirement is the capability to detect γ-radiation with $100\,\text{keV} \lesssim E_\gamma \lesssim 30\,\text{MeV}$ and light charged particles, mainly protons, with energies of up to $E_p \lesssim 700\,\text{MeV}$. Three different operation modes are defined for *CALIFA*:
As a high-resolution spectrometer low-energy γ rays with $0.1 - 2\,\text{MeV}$ and low multiplicity have to be detected. The desired energy resolution is required to be at least $\Delta E_\gamma \approx 60\,\text{keV} \cdot \sqrt{E_\gamma[\text{MeV}]}$.
Another case uses *CALIFA* as a γ ray calorimeter for the measurement of high-energetic γ rays with up to 10 MeV. In addition high-multiplicity events have to be detected. The intrinsic photopeak efficiency is therefore the key parameter to measure the correct γ ray sum energy and multiplicity.
A third case uses *CALIFA* as a hybrid detector, providing simultaneously high-resolution spectroscopic and calorimetric properties. In this most challenging scenario high-energetic light charged particles as well as the γ rays from de-excitation of the residual fragment are detected. The resulting scientific requirements for these three operation modes are an energy resolution of at least $\frac{\Delta E_\gamma}{E_\gamma}(1\,\text{MeV}) \lesssim 6\,\%$ for γs and $\frac{\Delta E_p}{E_p}(100\,\text{MeV}) \lesssim 1\,\%$ for high-energetic charged particles stopped in the active material [3]. Taking the Doppler shift of the γs into account, a constant energy resolution over the full detector requires a varying angular segmentation. To

accommodate these challenging requirements, the highly segmented structure of *CALIFA* is partitioned into three functional main parts (see figure 1.4).

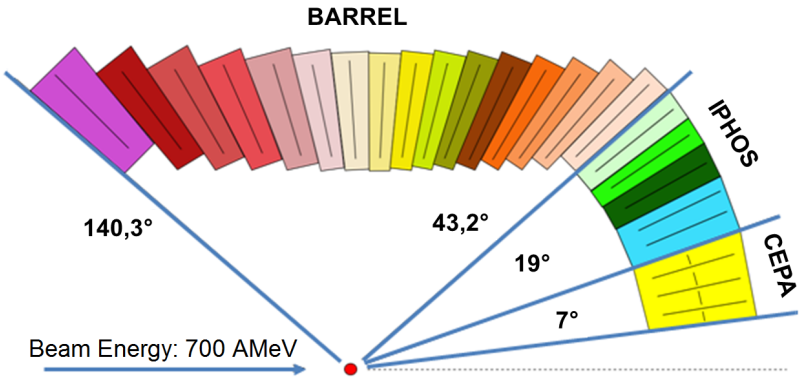


Figure 1.4: Partition and segmentation of *CALIFA*. Image taken from [6]

1.2.1 Barrel

The *Barrel* part covers an angular range from 43.2° to 140.3°. In this region the lowest energies and intensities for particles as well as for γ-rays are expected. Due to the strongly varying Doppler-shift of the γ-radiation the crystals of the *Barrel* differ strongly in their geometry to guarantee a correct reconstruction of the emission angle. 1952 Thallium doped Cesium-Iodide (CsI(Tl)) scintillation crystals are arranged in rings of 64 crystals each. Only the most backward ring consists of 32 crystals. The crystal lengths are chosen corresponding to the expected maximum energy deposit. Under a polar angle of $\Theta = 43.2°$ protons of $E_p \lesssim 320$ MeV shall be stopped. This corresponds to the maximum crystal length of 220 mm, which decreases to 150 mm at the largest polar angles of $\Theta = 143°$ [6].

1.2.2 Intrinsic Phoswich

The *Intrinsic Phoswich* section (*iPhos*) covers an angular range from $19° \leq \Theta \leq 43.2°$. It consists of 512 CsI(Tl) crystals with a length of 220 mm each. Protons emitted into the *iPhos* part have an additionally increased energy due to their Lorentz-boost. Particles with energies larger than $E \gtrsim 320$ MeV are therefore no longer stopped in the active material. Instead they punch through the crystals and deposit only a part of their full energy in CsI(Tl). A specially developed iPhos technique [7] based on a pulse shape analysis (PSA, see 2.3) however allows the identification and reconstruction of punched through particles. The event rate per crystal in this region is expected to be less than 1 kHz/crystal even at the highest interaction rates the spectrometer is designed for.

1.2.3 CALIFA Endcap Phoswich Array

The ***CALIFA Endcap Phoswich Array*** (*CEPA*) reaches from the most forward angles $\Theta \geq 7°$, defined by the opening angle of the dipole magnet *GLAD*, to $\Theta = 19°$. As the most forward part of *CALIFA*, it will see the highest rates of reaction products but also suffers from a large background from reactions in the upstream material from the beamline detectors. This master thesis focuses on the readout of the CEPA part. The design details and the experimental concept of the CEPA is therefore described in detail in the following chapter.

Chapter 2

The Califa Endcap Phoswich Array (CEPA)

CEPA is built up of 96 crystal pairs of cerium doped lanthanum bromide ($LaBr_3$) and lanthanum chloride ($LaCl_3$) in a phoswich configuration (see 2.1). The inner layer is made of 7 cm thick $LaBr_3$(Ce) crystals, the outer layer of 8 cm thick $LaCl_3$(Ce), optically coupled together. CEPA consists of four tapered rings, which are divided into eight segment units with 12 crystals each (see figure 2.1). Due to the highly hygroscopic character of the scintillation materials, each unit is encapsulated in a gas tight, 0.5 mm thick aluminum can. The crystals of one unit are optically insulated between each other by layers of reflective material.[1] The 4 mm thick exit window is also divided into 12 sub-windows to allow for an independent readout of each crystal-pair. One such pair has an exit surface of approximately 50x30 mm^2, which is readout by a single Hamamatsu R7600U-200 photomultiplier-tube with a sensitive area of $18 \times 18\,mm^2$ [8]. These metal package photo tubes are already resistant to the magnetic stray field of GLAD without additional shielding [3].

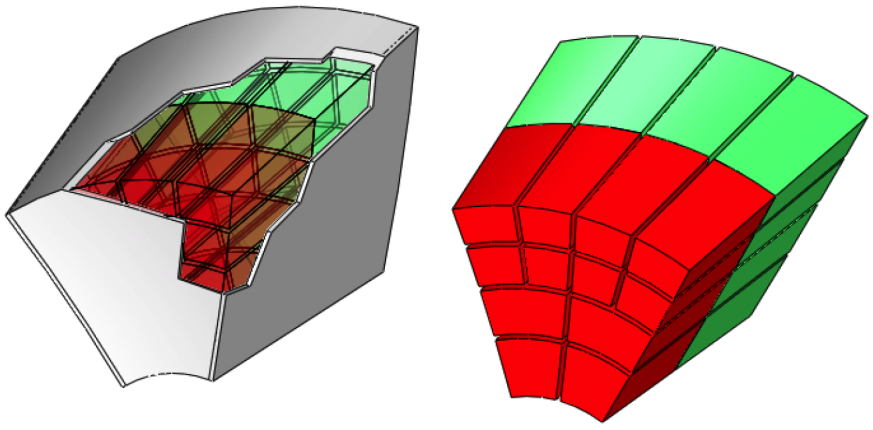


Figure 2.1: One CEPA segment, consisting of 12 crystal pairs, encapsulated in a single aluminum can. The inner layer (red) is built up of $LaBr_3$(Ce), the outer layer (green) of $LaCl_3$(Ce) crystals. The picture was taken from [3].

[1] no details provided by the producer St. Gobain

2.1 Phoswich

The basic principle of the phoswich-concept was described by D. H. Wilkinson already in 1952 [9]. He demonstrated the possibility to couple two different "oscillators" (phosphors) optically together in a sandwich-like structure and read them out with a single photomultiplier. The reconstruction of the different signal amplitudes allows for a wide range of applications. Also the name "phoswich" was a creation of Wilkinson, coming from the combination of "phosphors" and "sandwich".
In *CEPA* γs of up to 30 MeV and high-energy protons and other light-charged particles have to be detected to determine their energy. To understand the superior advantages of the phoswich-concept, one has to take a closer look on the possible interactions.
Low-energy γs entering a scintillator will either interact with the detector material by Compton scattering, depositing only a part of their full energy, or will be absorbed due to the photoelectric effect. A single crystal can not distinguish between those two interactions, whereas in a phoswich the absorption of a γ in the first crystal can be identified. The application of different veto conditions allows to increase the ratio of photopeak to Compton background for γ-radiation [10].
The interaction of high-energy γs in the scintillation material is however dominated by pair creation. To measure the full energy of the incoming γ-rays all reaction products of the resulting cascade have to be detected. Therefore, the first crystal of a phoswich has to be long enough to absorb most of the energy of the generated particles. No or at least only a small energy deposition in the second crystal is a hint for the full energy absorption of the initial γs. Also the specific pattern of additional spatially separated $E_\gamma = 511$ keV γ-rays from the pair annihilation allows for a sensitive event reconstruction.
A completely different interaction mechanism is present when a proton traverses through the phoswich. Protons experience a continuous slow down in the material, basically described by the Bethe-Bloch equation for energy loss of charged particles in matter. Here the specific energy deposit in first order depends on the particle's effective charge Z and its relative velocity $\beta = \frac{v}{c}$:

$$\frac{\mathrm{d}E}{\mathrm{d}x} \propto \left(\frac{Z}{\beta}\right)^2 .$$

The resulting characteristic curve for the energy deposition is shown in figure 2.2 for a massive block of material at constant density. Most of the energy of the proton is deposited in the so called Bragg-peak just before the particle is stopped. One way to measure the full energy of incoming protons is therefore to use long crystals to stop the protons in the entire active material. However, the chance for a loss in the measured energy due to nuclear reactions generating neutral particles and also dissipating binding energy in the scintillator increases with the length. A phoswich configuration offers a more suitable solution to measure the energy of high-energy protons with even shorter crystals. The initial energy is connected to the ratio of the energy deposited in the first and the second crystal and can be reconstructed even for punched-through protons. The basic advantages of the phoswich concept are the compact structure without any dead layers and the readout with only one device. To determine the different energy depositions from both materials, the corresponding contributions to the overall scintillation light have to be distinguished. Therefore four basic requirements have to be fulfilled for the two scintillation materials [10]:

- **Differentiate the scintillation light**
  The common way to separate the different scintillation lights is to use scintillators with sufficiently different characteristic decay times. The procedure for the separation is described in section 2.3. The contributions could also be separated by using scintillators

with different emission wavelengths λ, but this requires two readout devices at the end of the phoswich combination.

- **Transparency**
  The second crystal has to be transparent for the characteristic emission wave length of the first crystal and vice versa. Otherwise the mutual absorption of the scintillation lights with subsequent emission would falsify the reconstructed energy and make any conclusions on the detected particle impossible.

- **Similar physical properties**
  The direct coupling of the two scintillators results in the necessity of similar physical behaviour of the materials. A large difference in the refractive index introduces total reflection at the interface of the crystals, whereas different thermal properties as the thermal expansion ceofficient lead to tension in the material. Over that a common readout with a single photomultiplier requires the light output of both crystals to cover a similar wavelength region.

- **Similar light output**
  For a good separation of the different scintillation signals, the light outputs of both materials have to be similar. Otherwise a high light output (N) of one crystal will result in a high noise level ($\propto \sqrt{N}$), which covers any low light output from the second crystal.

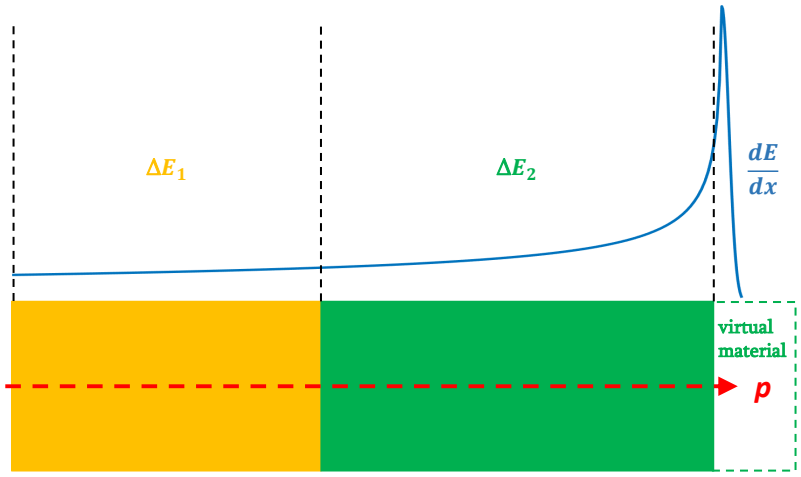


Figure 2.2: Schematic energy loss of a proton in a phoswich detector. The blue curve indicates the deposited energy along the path through a massive block of material at a constant density. In this example the proton punches through the two scintillation crystals, so that the full Bragg-peak is not absorbed inside the second crystal. Instead there is no further energy deposition in the virtual material but the proton exits the phoswich with the remaining energy.

2.2 $LaBr_3(Ce)$ and $LaCl_3(Ce)$ combination

Innovative inorganic scintillation materials have been a major field of research over the past decade. With an increasing demand in high-energy physics and medical imaging, a multitude of new scintillators were developed recently [10, 11].
A subset of selected scintillation materials is compared to traditional materials regarding their

main properties in table 2.1. Scintillator crystals with a high intrinsic resolution are required to ensure the desired energy resolution proposed in *CALIFA*. This is connected to a high light yield, which enables also the detection of low-energy γs with a sufficient resolution. Due to the position of the *CEPA* detector in the most forward direction of *CALIFA*, highest rates are expected. To avoid pile-up effects a fast detector signal with a short decay time is desired. On the other hand the decay times of the two phoswich crystals must have a sufficient difference for a precise separation using the pulse shape analysis. In principle any combination of scintil-

	BGO	LYSO(Ce)	NaI(Tl)	CsI(Tl)	$LaBr_3$(Ce)	$LaCl_3$(Ce)
Density [g/cm^3]	7.13	7.1	3.67	4.51	5.08	3.85
Light yield [photons/keV]	$8-10$	32	38	54	63	49
$\lambda_{\text{max emission}}$ [nm]	480	420	415	550	380	350
Decay time τ [ns]	300	41	250	600, 3500	16	28
$\frac{\Delta E}{E}\big\vert_{662\,\text{keV}\,\gamma}$	9.7%	7.1%	7% [12]	6% [12]	2.9%	3.8%
Hygroscopic	no	no	yes	slightly	yes	yes

Table 2.1: Selected characteristic properties of different scintillation materials according to [13].

lation materials can be used in a phoswich configuration. For example a study was carried out in 2013 by C. Pfeffer using CsI(Tl) together with Lutetium-Yttrium oxyorthosilicate (LYSO) [14]. A test with high-energy protons with energies of $E = 70 - 226$ MeV at the Bronowice Cyclotron Center in Krakow revealed only moderate energy resolutions for high energies, as well as the internal radioactivity of lutetium generates a high background for the measurement of low-energy γs. Another promising combination was realised in the *PARIS* detector using $LaBr_3$(Ce) and NaI(Tl) [15]. This setup showed a significant degradation of the energy resolution for high counting rates ($\frac{\Delta E}{E}\big\vert_{835\,\text{keV}\,\gamma} = 13\%$ at 150 kHz). To avoid this material effect the proposed solution was a separation of both materials by a passive layer of glass.
For *CEPA* cerium doped scintillators $LaBr_3$(Ce) and $LaCl_3$(Ce) were chosen to fit the scientific requirements best. With fast decay times of 16 ns for $LaBr_3$(Ce) and 28 ns for $LaCl_3$(Ce) [16, 17] those scintillators allow a high counting rate as well as a good time resolution. Especially for low energy γ-rays $LaBr_3$(Ce) still provides an unprecedented resolution (see table 2.1). Materials like SrI2 with similar properties are still in a very early stage of development and not yet produced in sufficient quantities and sizes. Due to their emission peaks at 380 nm for $LaBr_3$ and 350 nm for $LaCl_3$, these scintillators can be read out by a single photomultiplier. *CEPA* will use the photomultiplier-tube (PMT) R7600U-200 from Hamamatsu. The spectral response of this PMT is shown in figure 2.3. With a maximum sensitivity at 400 nm, which is nearly constant over the range of $350 - 450$ nm, and a fast rising time of 1.2 ns it is suited for the readout of $LaBr_3$ and $LaCl_3$ [18]. The typical gain of 10^6 provides clear signals even for γ energies around a few keV. The combination was already tested at the Instituto de Estructura de la Materia (IEM) in Madrid and at The Svedberg Laboratory (TSL) in Uppsala [19]. The used demonstrator detector consisted of a 30 mm thick $LaBr_3$(Ce) and a 50 mm thick $LaCl_3$(Ce) crystal. Tests with low-energy γs with 662 keV standard sources showed an energy resolution of 4.5%. High-energy protons from TSL with energies of up to 180 MeV could be detected with an energy resolution of $\frac{\Delta E}{E} \leq 1\%$.

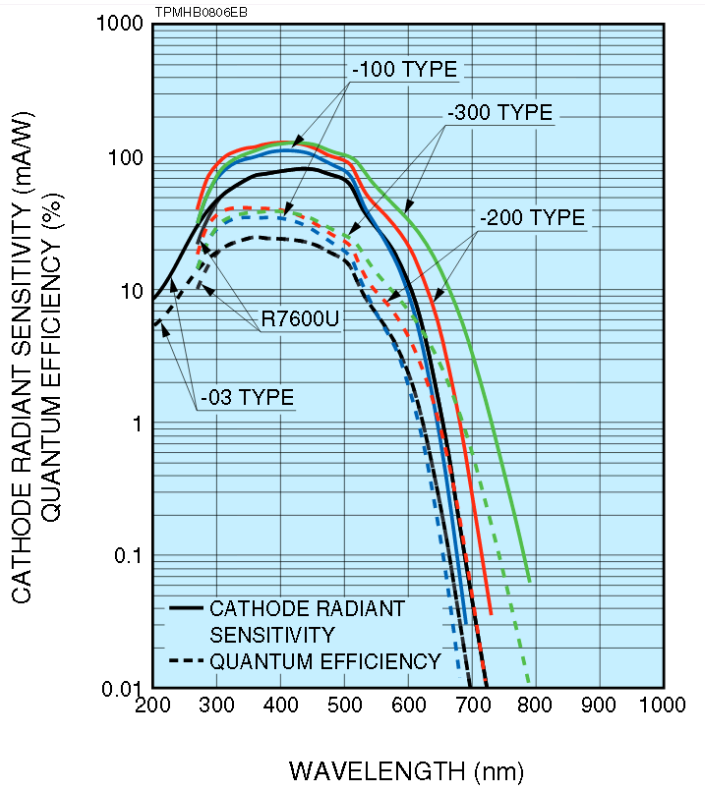


Figure 2.3: Spectral response of Hamamatsu R7600U-200 PMT in red. The dotted red line represents the corresponding quantum efficiency. The diagram is taken from [18].

2.3 Pulse-Shape-Analysis

The readout of a phoswich with one single photomultiplier results in an effective signal which superimposes the two different light output curves. The luminescence signal L is therefore given as the sum of two independent exponential decays with the characteristic decay times τ_1 and τ_2 of the scintillation materials:

$$L(t) \approx \frac{N_1}{\tau_1} e^{-\frac{t}{\tau_1}} + \frac{N_2}{\tau_2} e^{-\frac{t}{\tau_2}}$$

N_1 and N_2 describe the total numbers of electrons of the PMT output for each scintillation component. The rise times of the signals $\tau_r \ll \tau_{1,2}$ are much faster than the decay times and can therefore be neglected. To reconstruct the energy of any stopped or even punched-through particle, those contributions have to be separated and the different signal amplitudes calculated. A common way to do so is to integrate the signal in two time windows [20], one right at the beginning of the signal and another one after some time. Using appropriate window sizes the integrated charges from the first window are dominated by the light output of the faster crystal, while the charge collected in the delayed window contains a larger fraction of the signal produced by the slower crystal. A larger difference between the two decay times improves this reconstruction method, which is described in detail in section 3.1.2.
But even though the decay times of $LaBr_3(Ce)$ and $LaCl_3(Ce)$ are quite similar a pulse shape analysis allows to separate the two amplitudes of the scintillation light. Figure 2.4 shows a spectrum of measurements with high-energy protons up to $E = 220\,\text{MeV}$ using the *CEPA* demonstrator mentioned before. The measured energies from the $LaBr_3$ versus the full deposited energy describes for lower proton energies a bisectrix, as all protons are stopped in the first crystal. For increasing energies only a part of the energy is deposited in the first crystal,

while the other part is detected in the $LaCl_3$ crystal. At last punched-through protons deposit again less energy in the second crystal due to the absent Bragg-peak.

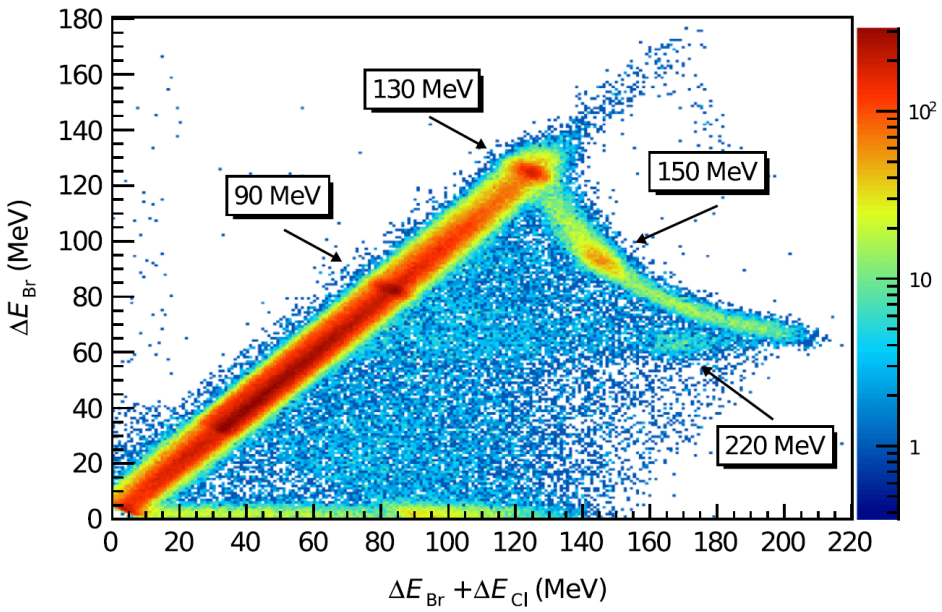


Figure 2.4: Reconstructed energy deposition in $LaBr_3$ over the full energy in $LaBr_3$ and $LaCl_3$ from a test run at the Bronowice Cyclotron Centre in Krakow. Protons with an energy of up to 130 MeV are fully stopped in the $LaBr_3$ crystal. For higher energies the protons punch through the first crystal and are stopped in the $LaCl_3$. Incoming protons with more than approximately 200 MeV are no longer stopped in neither of the crystals, the resulting ratio of the deposited energy allows a reconstruction of the initial energy however. Plot taken from [21].

Chapter 3

The Fully Digital Readout Concept of CALIFA

The *CALIFA* detector is divided into three structural parts with different technical and physical requirements in order to reach the intended detector performance. As a result the Barrel, iPhos and CEPA part differ in the geometry and the choice of the scintillating material, as well as in the readout of the detection units. A homogeneous data acquisition system with mostly identical modules and algorithms is however desired. Using a fully digital system transforming the analog input signals into digital ones right after the preamplifiers enables the possibility to adapt the digital processing of the signals to the requirements with a high flexibility. Thereby the effort in development, maintenance and operation of the whole system is minimized. For the *CALIFA* calorimeter this concept is based on the FEBEX 3B Digitizer with a real-time signal processing firmware implemented. A diagram of the data acquisition system shown in figure 3.1 illustrates the hardware layout. In the following the fully digital readout concept of *CALIFA* will be illustrated based on the existing CsI(Tl) scintillators in the Barrel and iPhos part, before the challenges and necessary changes for $LaBr_3$(Ce) and $LaCl_3$(Ce) of the *CEPA* are discussed.

3.1 CsI(Tl) readout

The readout of the *Barrel* and *iPhos* parts are divided in three functional stages: charge integrating amplification of the scintillation signals from the APD-sensors, digitization of this signal and pulse shape analysis implemented in the hardware. In the following the most important electronic components for the readout are explained in detail.

3.1.1 Readout electronics

Preamplifier After the scintillation light was detected in the Hamamatsu S8664-1010 Large Area Avalanche Photo Diode (LAAPD), the resulting signals of 32 channels are processed by the charge sensitive preamplifier MPRB-32 (or MPRB-32-DR for the *iPhos* part) developed by Mesytec[2]. These preamplifiers were developed especially for *CALIFA* and provide high voltage supply with gain stabilization for the individual APDs, remote control capability and two gain stages for energy ranges of $E \leq 30\,\mathrm{MeV}$ and $E \leq 300\,\mathrm{MeV}$. Each module consists of 32 independent charge-integrating preamplifiers with a decay time of $\tau_D \approx 35\,\mu\mathrm{s}$ [20], which leads to a ballistic deficit in the preamplifier signal and has to be digitally corrected. In the MPRB-32 version 32 channels are amplified with one of the two available gains. In contrary,

[2]mesytec Detector Readout Systems, www.mesytec.com

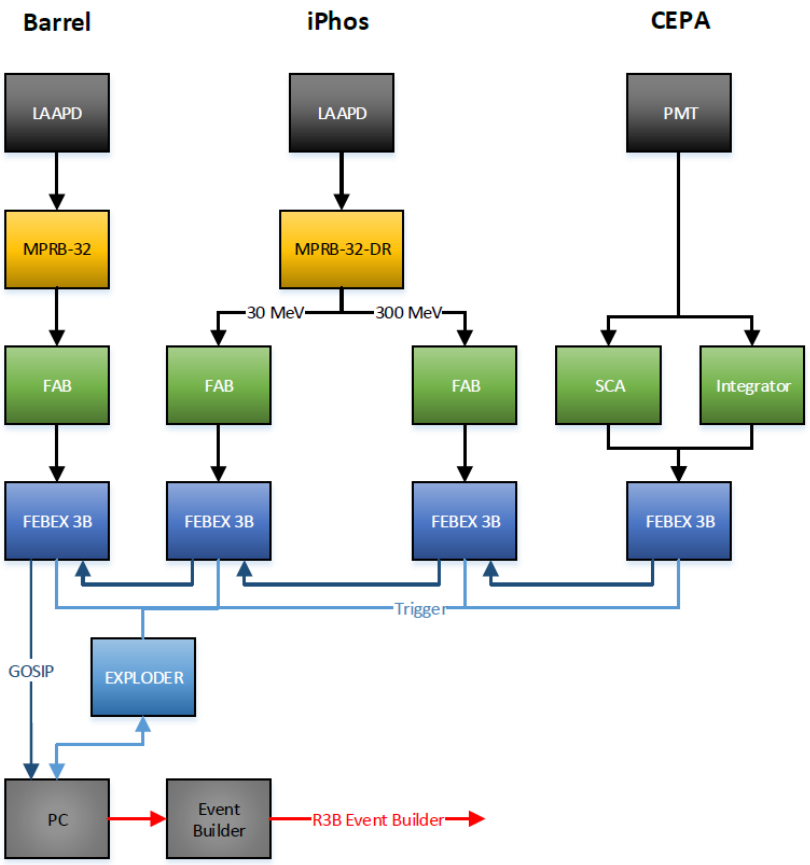


Figure 3.1: Scheme of the data acquisition system for *CALIFA*, taken from [20]. The CsI(Tl) scintillators in the *Barrel* and *iPhos* part of *CALIFA* are read out by Hamamatsu S8664-1010 Large Area Avalanche Photo Diodes (LAAPDs). The signal is then amplified in the MPRB-32 and MPRB-32-DR preamplifier, respectively. Analog signal corrections are performed on the FEBEX Add-on Board (FAB), before the traces are digitized on the FEBEX3B boards. For the *CEPA*, the crystals are read out by Hamamatsu R7600U-200 photomultiplier tubes. The signals will be preprocessed on the add-on board, developed in this thesis, before it becomes digitized as well. The whole setup is controlled by a PC system, which combines the different signals to an event.

the MPRB-32-DR version processes also 32 channels in the same way, but splits each signal so both gain stages are used in parallel. A remote control system allows the adjustment of the high voltage for each channel individually, while the configurable temperature compensation affects commonly packages of 16 channels.
The output signals of the preamplifiers are differentially transmitted to the FEBEX Add-on Board via 34 wire shielded twisted pair cables.

FEBEX 3B Central part of the digital readout is the *Front End Board with optical link EXtension* revision 3B (FEBEX3B), developed by GSI (figure 3.2). Two differential 14 bit sampling *Analog-Digital-Converters* (ADCs) with eight channels each and a sampling rate of 50 Ms/s digitize the analog input signals. The data are fully digitally processed and analyzed in a Lattice ECP3-150 Field Programmable Gate Array (FPGA). The firmware of this component was a special development of the working group at the Technical University of Munich (TUM) [10, 20] and is described in section 3.1.2. A connection for add-on boards is available

via a Samtec connector with 16 differential pairs directly connected to the ADCs and 16 differential pairs connected to the FPGA. The latter ones can be driven in a LVDS standard or operated individually as single-ended connectors. A PCIe connector with four serial 1.6 Gbit/s connections is used for power supply and communication via GOSIP protocol, as well as an additional MLVDS bus with eight lines for trigger distribution. Up to 20 of such modules can be placed in a 19 inch crate with common Small Form-factor Pluggable (SFP) for control and readout of all boards. The MLVDS trigger bus of one crate is linked to an EXPLODER (trigger distribution module, described in the following) via a 28 pole mini ribbon cable.

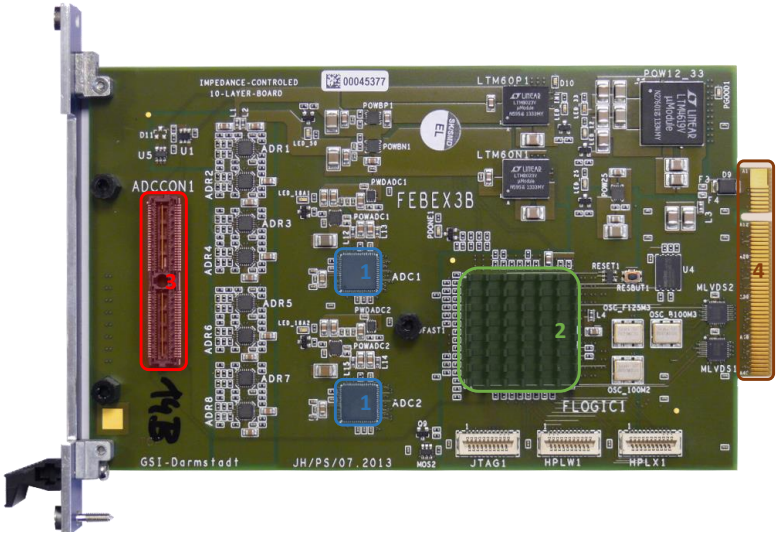


Figure 3.2: FEBEX3B board developed by GSI Electronic Department [22]. (1) two differential 14 bit sampling ADCs with 8 channels each and a sampling rate of 50 MHz (2) Lattice ECP3-150 FPGA (and mounted cooling element) with implemented firmware for a pulse shape analysis (3) 104-pole connector to mount add-on boards (4) connection to the backplane for global trigger-bus and readout

FEBEX Add-on Board (FAB) The FEBEX Add-on Board, which was developed in Munich [20], fulfills two main functions:
According to the *Nyquist-Shannon* sampling theorem only such signal frequencies can be correctly digitized, which are lower than half the sampling rate. Any higher frequency component will be misinterpreted and leads to aliasing [23]. The FEBEX board digitizes the signal with a sampling rate of 50 Ms/s. Therefore the signal from the preamplifiers has to be filtered to have a preferably sharp cutoff-frequency of 25 MHz and the signal should not be deformed in the accepted transmission band. An active two-pole Bessel-filter is used on the FAB to filter out high frequency with a cutoff frequency of $f_{3dB} = 16$ MHz [20].
The second task of the FAB is to shift the preamplifier signal with a DC-offset to fit the input range of the Analog-to-Digital Converters (ADCs) of the FEBEX board. With a purely positive output of the preamplifier and a input range of ± 0.9 V of the ADCs, only part of the available resolution could be used. Through shifting the signal with an individual offset the negative range and therefore the full ADC range is used. The height of the applied DC-offset is regulated by digital potentiometers, which are controlled by the FEBEX board.
All operating voltages of the FAB have to be generated on the board since only a 12 V power supply is present from the FEBEX board. For the positive operating voltages (1 V, 3.3 V) linear regulators are used for minimizing the noise. For the negative operating voltage of -2 V the step down regulator LTM8023 with a LC-filter for decoupling is used and shielded by a

metal cage. Corrected output signals of the FAB are transmitted to the FEBEX3B board via a Samtec-connector.

EXPLODER The EXPLODER-module developed by GSI is used for trigger distribution. The MLVDS trigger busses of up to four PCIe crates are connected to one EXPLODER. Two separate plugs for in- and output in Emitter Coupled Logic (ECL) standard connect the EXPLODER to the readout PC. An on-board XILINX Spartan 6-150 FPGA provides programmable input- and output matrices. Those matrices can link inputs, internal pulse-generators and outputs in any order and are adjusted via slow control from a PC. For physical trigger lines a dead-time-blocker is implemented internally, while other triggers, e.g. for trigger counting, are routed around the dead-time-blocker.

3.1.2 Digital pulse shape analyzer

The dead-time free, online signal processing firmware of the FEBEX FPGA was especially developed for *CALIFA* [20]. A Quick Particle IDentification (QPID) algorithm and the reconstruction of energy depositions are implemented and build up an event. The firmware can be used in two different operating modes:

1. *single-event readout*: The recorded data is read out immediately after an accepted trigger. An implemented bank switching still allows to record data without additional dead time if less than two triggers occure within the readout time.

2. *multi-event readout*: Recorded events are stored in the module until an adjustable number of events was gathered. Bank switching and block readout allow a fully dead time free readout.

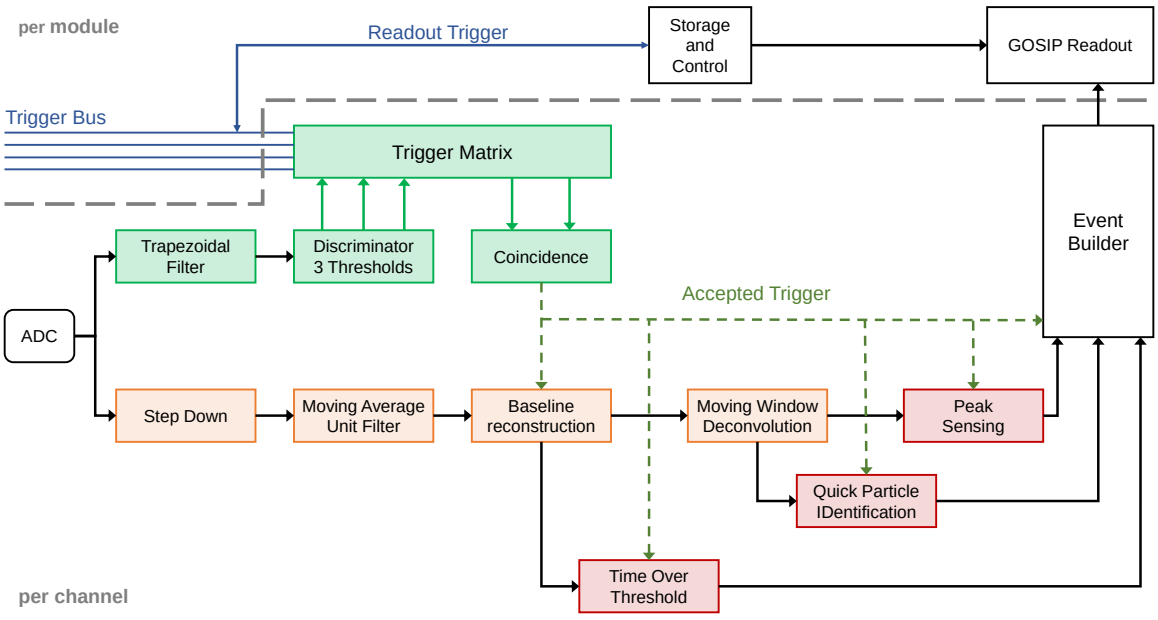


Figure 3.3: Schematic overview of the firmware for FEBEX3B, adopted from [20]. The signal from the ADC is split into two different paths. In a fast time-path (green) readout triggers are generated, while in a slower energy path (orange/red) the signal is evaluated in detail (e.g. energy, particle identification,...).

Figure 3.3 shows an overview of the firmware. The digitized signal from the ADC is split into two branches. In the *time-path* the signal is smoothed out by a fast trapezoidal filter for a better signal-to-noise ratio and differentiated with adjustable time constants. Three leading edge discriminators with different thresholds generate triggers which are transmitted to a programmable trigger matrix. The configuration of this trigger matrix defines the current operation mode:

1. Either each channel works with an own, independent trigger on either of the trigger signals or

2. all channels are controlled by a single trigger signal from selected channels.

It is also possible to check each channel for a coincidence with a generated trigger and read out only in case of a positive result. The trigger-matrix of each channel is therefore connected via an internal trigger bus to the other channels and to trigger signals from the EXPLODER. Due to the slow response of CsI(Tl) crystalls, in the *energy-path* the signal rate is decimated to 25 Ms/s by summation of two consecutive samples. This allows an online handling of four channels with the 100 MHz processing frequency of the FPGA in a single unit. The decimated signal is delayed to compensate for the transit time generation of a trigger in the time-path. After that a Moving Average Unit (MAU) of variable length filters the signal by averaging the noise. The baseline of the waveform is reconstructed and subtracted from the input signal. To get the integral charge signal of the scintillation process, the decay-time of the preamplifier has to be removed. This is done by a Moving Window Deconvolution (MWD). The maximum pulse height of the resulting signal is proportional to the full deposited energy in the crystals. The different scintillation amplitudes N_1 and N_2 of the fast and the slow decay of CsI(Tl)'s scintillation light are separated in the QPID algorithm, which is described later in detail, and allows the identification of the detected particles.
While all signal processing filters are executed continuously for an unbuffered online signal processing, the analysis (peak sensing, TOT, QPID) is only performed when a valid trigger occurs. The timestamp, pulse height and scintillation amplitudes are linked in the event builder as one event. This data is then read out via the GOSIP protocol to the connected readout PC. It is also possible to monitor the signal trace between every processing step to optimize and adapt the algorithms to the active signal shape.
For a better understanding of the different processes and required changes for the $LaBr_3$ and $LaCl_3$ readout, the underlying algorithms are explained in the following.

Discriminator The digitized signal from the ADC is smoothed by a square filter before it is used for trigger generation.

$$Q_i = \sum_{k=i-L}^{i} U_k - \sum_{k=i-L-G}^{i-G} U_k \tag{3.1}$$

All sampled amplitudes inside a time window of length L are summed up to smooth the signal and the derivative is calculated by subtracting two summed values from windows shifted by the time G. A short value for G reduces the pulse length and prevents therefore pile-ups and the missing of events.
Three leading-edge discriminators with configurable thresholds generate the readout triggers. A low threshold of $E \gtrsim 50$ keV is used for fast timing triggers, while a γ trigger with $E \gtrsim 100$ keV and a proton trigger of $E \gtrsim 10$ MeV are used to distinguish between typical events. The coincidence of the timing trigger with the γ triggers of several channels gathers the full energy deposition of γs in multiple crystals.

Moving Average Unit filter (MAU) A Moving Average Unit filter is applied to the signal in the energy-branch to filter out any high-frequency noise and smooths the signal. Therefore all amplitudes U_k inside a time window of Length L in sampling times are summed up and divided by L.

$$U_{i\,\mathrm{MAU}} = \frac{1}{L} \sum_{k=i-L}^{i} U_k \tag{3.2}$$

This way the mean value inside the window is calculated, which reduces the effect of noise. The longer the time window, the smoother the signal becomes, but the signal shape might also be deformed. The time window is chosen as a compromise between the filtering of high-frequency noise and the maximum of the light curve detected.
In a subsequent step the baseline of the signal is reconstructed using a modified MAU filter. As mentioned before, the FAB adds a DC-offset to the signal to use the full input range of the ADCs. This offset and any other shifts like low-frequency noise are compensated by subtracting the mean value in a long time window before the event happened. The calculation of this mean value is stopped for a certain dead time whenever a trigger occurs. This way a signal pulse decays without shifting the reconstructed baseline.

Moving Window Deconvolution (MWD) At this segment in the firmware analysis the signal represents the baseline corrected and smoothed output of the preamplifier. As mentioned in section 3.1.1, the preamplifier integrates the scintillation signals and decays with an instantaneous decay time of $\tau_D = 35\,\mu$s. The resulting signal $U(t)$ is given as the convolution of the luminescence signal $L(t)$ (see 2.1) and the exponential decay $D(t)$ of the preamplifier. The Heaviside function $\Theta(t)$ describes the restriction in time to positive values.

$$U(t) = \int_0^t L(t') \cdot D(t - t')\,\mathrm{d}t' \tag{3.3}$$

$$= \Theta(t) \cdot \left[\frac{N_1 \tau_D}{\tau_D - \tau_1} \cdot \left(\mathrm{e}^{-\frac{t}{\tau_D}} - \mathrm{e}^{-\frac{t}{\tau_1}} \right) + \frac{N_2 \tau_D}{\tau_D - \tau_2} \cdot \left(\mathrm{e}^{-\frac{t}{\tau_D}} - \mathrm{e}^{-\frac{t}{\tau_2}} \right) \right] \tag{3.4}$$

This results in two effects. On the one hand two events in rapid succession will overlap, as the second event will occur before the preamplifier signal of the first one is fully decayed. The pileup of those events leads to an increased signal amplitude and therefore to an overestimation of the measured energy. On the other hand the instantaneous decay of the preamplifier signal prevents from a full integration of the scintillation signal. The signal height is underestimated, a so called ballistic deficit occurs. In order to reconstruct the integrated scintillation signal and reduce the pile-up effect a Moving Window Deconvolution (MWD) algorithm, introduced by [24], is used. It assumes a discrete convolution of a temporary charge signal with a single exponential decay. The MWD algorithm then reconstructs the charge signal inside a window of L sampling points, which is moved over the raw preamplifier signal. The equation for the reconstruction is given by:

$$Q_i = U_i - U_{i-L} + (1 - \mathrm{e}^{-\Delta t/\tau_D}) \sum_{j=i-L}^{i} U_k \approx U_i - U_{i-L} + \frac{\Delta t}{\tau_D} \sum_{j=i-L}^{i} U_k \tag{3.5}$$

U_i is the voltage of sample i, Δt the sampling time, τ_D the decay time of the preamplifier, L the MWD window size in multiples of the sampling time and Q the deconvoluted charge signal. The algorithm calculates the charge added to the signal inside the MWD window. To get the full integration of the charges generated in one event as maximum, the window size has to include the whole scintillation signal. Assuming also an exponential decay for the scintillation signal with two time constants $\tau_{1,2}$ as in 2.1, the integrated charge when the MWD window overlaps

completely with the raw signal corresponds to approximately $Q_{\mathrm{MWD}}/Q_{abs} \approx 1 - \exp(-L\frac{\Delta t}{\tau_{1,2}})$ of the absolute charges. After that the deconvoluted signal decays strongly, limiting the critical time for pile-up effects.
An exemplary CsI luminescence signal with a fast and a slow decay component is depicted in figure 3.4 in black. The preamplifier integrates that signal and decays with a much longer decay time, thus producing the typical shape of the red curve. The MWD algorithm is applied in a time window of 35 us, i.e. more than 99.99% of the charges from the scintillation signal are summed up. The deconvoluted MWD-signal $Q(t)$ is plotted in green. As can be seen, the maximum amplitude of this curve is higher than the maximum of the preamplifier signal due to the ballistic deficit (blue). Beyond that, the signal decays strongly after one window size, reducing the probability of a pile-up.

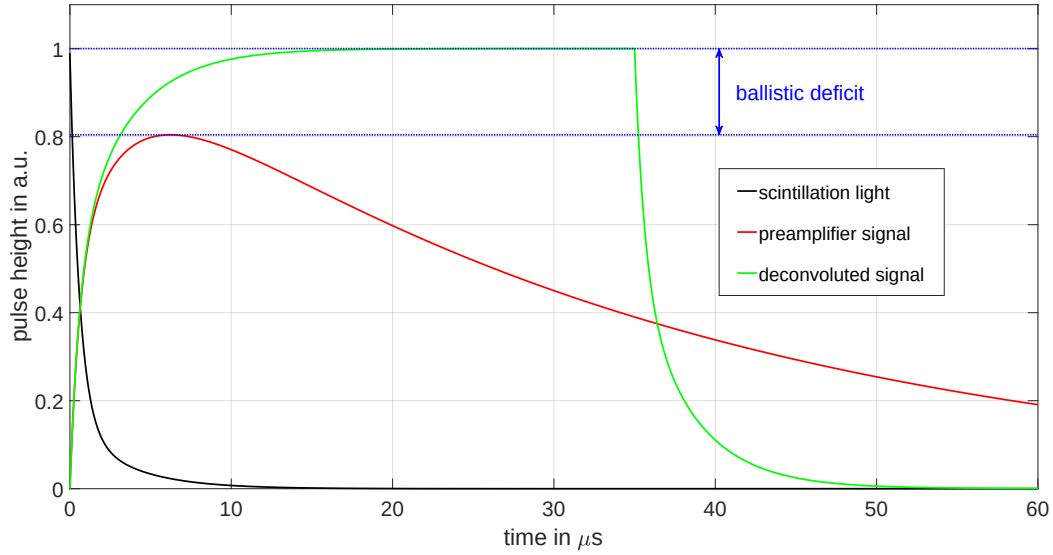


Figure 3.4: Comparison of the preamplifier signal (red) for CsI(Tl) and the deconvoluted, integrated scintillation signal after the MWD (green) for CsI(Tl). The ballistic deficit (blue) due to the decay of the preamplifier signal has been removed and the signal length shortened to reduce pile-ups by choosing a time window of 35 μs.

Quick Particle IDentification (QPID) The MWD reconstructs the integrated charge signal $Q(t)$ of the scintillation, which is of the form

$$Q(t) = \int_0^t L(t')\,\mathrm{d}t' = \Theta(t) \cdot \left[N_1 \cdot \left(1 - \mathrm{e}^{-\frac{t}{\tau_1}}\right) + N_2 \cdot \left(1 - \mathrm{e}^{-\frac{t}{\tau_2}}\right)\right]. \tag{3.6}$$

The two amplitudes N_1 and N_2 of the different scintillation processes have to be determined to calculate the deposited energy in the scintillation crystal. The Quick Particle IDentification (QPID) algorithm was developed especially for *CALIFA* by Max Winkel [25] and allows a resource effective online analysis of the measurements in the FEBEX FPGA. It uses the common approach to integrate the signal $Q(t)$ in two time windows at the beginning and the end of the MWD window, as depicted in figure 3.5. The following section summarizes the basic concept of the QPID from [25] for a better understanding and reading of this paper. With the antiderivative $F(t)$ of the integrated signal $Q(t)$, the contents $\hat{Q}_1$ and $\hat{Q}_2$ of the two

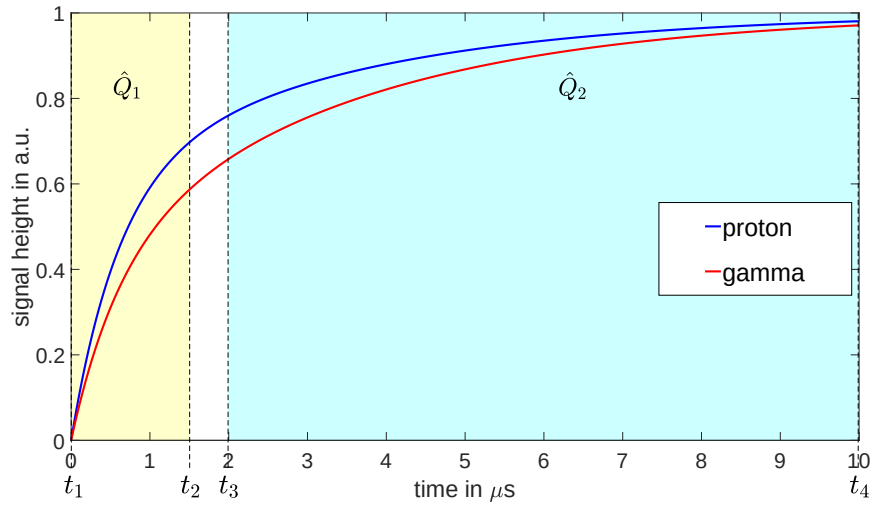


Figure 3.5: The concept of the QPID. The integrated charge signals after the MWD are integrated in two time windows, indicated in the shaded areas. The Integrals $\hat{Q}_1$ and $\hat{Q}_2$ are used to calculate the scintillation amplitudes N_1 and N_2 (following [25, 26]).

integration windows are given as

$$\hat{Q}_1 = F(t_2) - F(t_1) = A \cdot N_1 + B \cdot N_2, \tag{3.7}$$

$$\hat{Q}_2 = F(t_4) - F(t_3) = C \cdot N_1 + D \cdot N_2. \tag{3.8}$$

t_1 to t_4 describe the fixed boundaries of the windows, the values A, B, C and D describe the contributions of the different signal amplitudes N_1 and N_2 to the integrals. As these parameters only depend on the window boundaries and the decay times of the scintillation signals, they can be calculated independent of the actual measurement. The derivation of the actual values can be found in [20]. By inverting the linear equation system, N_1 and N_2 can be calculated from the integral contents $\hat{Q}_1$ and $\hat{Q}_2$.

$$\begin{pmatrix} \hat{Q}_1 \\ \hat{Q}_2 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \cdot \begin{pmatrix} N_1 \\ N_2 \end{pmatrix} \Leftrightarrow \begin{pmatrix} N_1 \\ N_2 \end{pmatrix} = \frac{1}{AD - BC} \cdot \begin{pmatrix} D & -B \\ -C & A \end{pmatrix} \cdot \begin{pmatrix} \hat{Q}_1 \\ \hat{Q}_2 \end{pmatrix}. \tag{3.9}$$

The ratio of the amplitudes N_1 and N_2 depends on the energy and also on the type of the detected particles [27]. Figure 3.6 shows the measurements of a test experiment at the Laboratori Nazionale del Sud (LNS) in Catania. A beam of ^{12}C with an eregy of $E = 80$ AMeV was directed on different targets. A combination of a CsI(Tl) scintillation crystal and a BC408 plastic scintillator was used as detector. The measured fast scintillation amplitude N_f versus the slow scintillation amplitude N_s are plotted in 3.6. The precise separation of the two components results in sharp bands for identicle particles. Higher amplitudes within one band corresponds to a larger energy deposition inside the scintillators. A detailed analysis of the experiment can be found in [20].

3.2 $LaBr_3(Ce)/LaCl_3(Ce)$ readout

As already mentioned in the beginning of this chapter, an homogeneous data acquisition system using a maximum overlap in hardware and firmware is desired for *CALIFA*. In the *CEPA* part of the detector the rather slow CsI(Tl) scintillation crystals are replaced by a phoswich

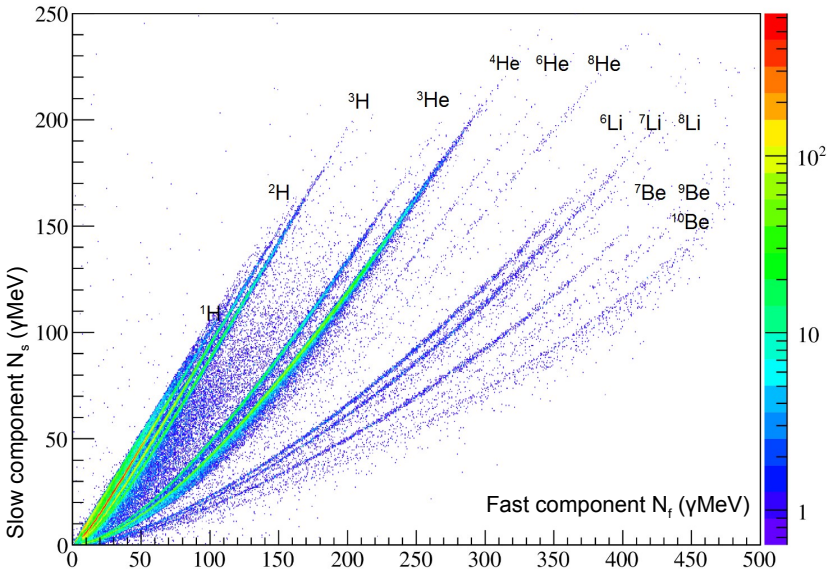


Figure 3.6: Data from a test experiment at the LNS in Catania. The scintillation amplitudes were calculated by the QPID algorithm. Each correlation band corresponds to one particle type. This plot was taken from [20].

combination of $LaBr_3$ and $LaCl_3$ crystals with much faster decay times of $\tau_{LaBr3} = 16$ ns and $\tau_{LaCl3} = 28$ ns, respectively. While the algorithms of the firmware stay valid and only their parameters have to be adjusted to the new signal, the fast decay of the scintillation pulses can not be handled by the ADCs any more. An exemplary $LaBr_3$ / $LaCl_3$ signal is depicted in figure 3.7. The effective signal output of the photomultiplier tube (blue) is given as the sum of those two components. When sampling the signal in the ADCs with a frequency of 50 MHz, one sampling point is measured every 20 ns (shaded areas). Thus, a full scintillation pulse is covered by only 4-5 data points; a separation of the two decay components for energy reconstruction and particle identification is not possible.
To increase the sampling speed for *CEPA* while simultaneously preserving the possibility of an online analysis and using the FEBEX 3B hardware an analogue preprocessing is performed. As a basic idea the PMT signal will be stored in a fast sampling switched capacitor array. Only when a trigger is generated, the data will be read out with a reduced speed. The development of a new add-on board for FEBEX, preprocessing and sampling the PMT output using a switched capacitor array, was the major task of this master thesis.

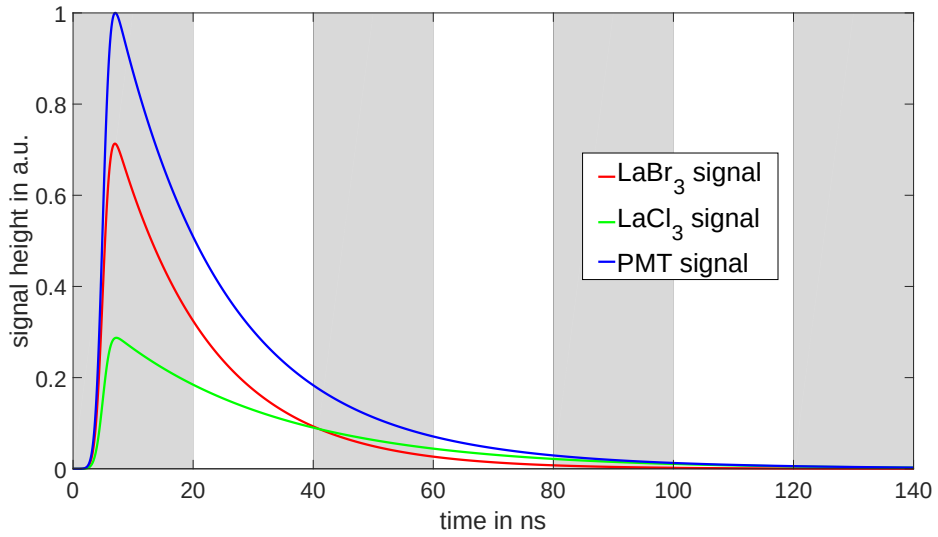


Figure 3.7: Data coverage of a typical *CEPA* signal using the FEBEX board with 50 MHz ADCs. The scintillation light of $LaBr_3$ (red) and $LaCl_3$ (green) is read out by a single photomultiplier, so the effective sum signal (blue) is present at the FEBEX input. ADCs sampling at 50 MHz take a data point every 20 ns (shaded areas). The time position of the signal is randomly distributed under real conditions.

Chapter 4

Hardware Development

The basic concept of a GHz sampling ADC for the *CALIFA* calorimeter is based on the FEBEX3B board from GSI and the newly developed DRS4 FEBEX Add-on Board (DFAB). The requirements for the add-on board are a low noise data sampling with 1 Gs/s to enable high resolution measurements of each crystal as well as a separate signal branch for trigger generation. A simple readout scheme of the board is depicted in figure 4.1.

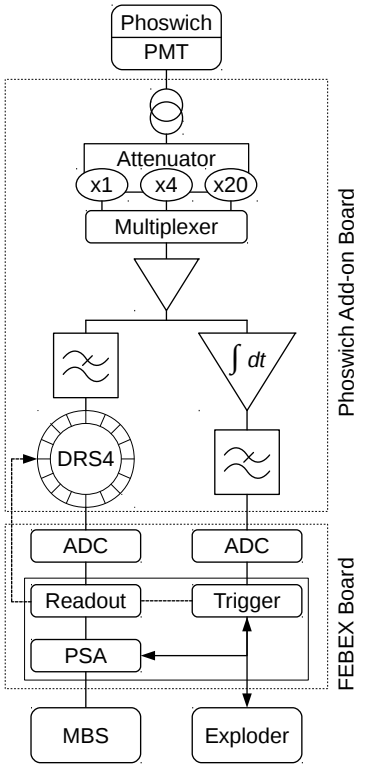


Figure 4.1: Readout-scheme for CEPA. The incoming PMT signal is attenuated and decoupled before is is split up into two branches. A readout trigger is generated on the FEBEX board on basis of the integrated PMT signal in the right branch. In the second branch, the fast sampling switched capacitor array DRS4 is used to store the signal shape until it is read out by the FEBEX board.

4.1 Mixed Analog-Digital System

For the reconstruction of the scintillation components of $LaBr_3(Ce)$ and $LaCl_3(Ce)$ the signal has to be sampled at high frequencies. As described in section 3.2, the existing readout system is not capable of digitizing the signal at a sufficient rate. Therefore the analog signal is divided into discrete packages, which are buffered and can then be read out in the case of a trigger with a reduced output frequency. This intermediate mixed analog-digital system is realized by a switched capacitor array, whose mode of operation is described in the following.

4.1.1 Switched Capacitor Array (SCA)

Basic principle of a switched capacitor array is to store an analog signal in a series of capacitors. The stored charge in each cell represents the input signal integrated in a short time window, defined by the switching time to the next cell. This continuous sampling is controlled by a specifically chosen external clock. In figure 4.2 a scheme of the operating principle is given. If the *Write* switches S_i are closed, the analog input signal will be stored in n capacitors

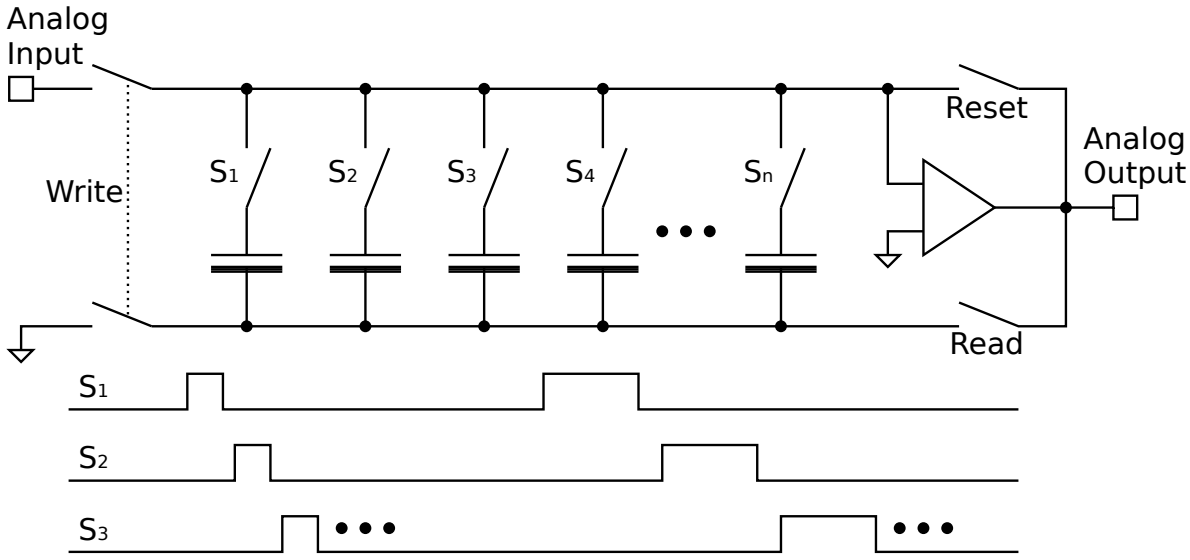


Figure 4.2: Operating principle of a Switched Capacitor Array (SCA). When the *Write* switches are closed, the input signal can be applied to any of the n sampling capacitors by activating the corresponding switch. During the sampling time t_{samp}, switch S_1 is closed and the signal is integrated in the first capacitor. The opening of S_1 and closing of S_2 continues this sampling in the second cell etc. This procedure is visualized in the exemplary signal curves of the switches S_1, S_2 and S_3. For readout, the *Write* switches are opened and the *Read* switch closed instead. A similar process as for the sampling is used to apply the stored voltage of each cell subsequently to the readout buffer. The time for each cell readout is increased $t_{\text{read}} > t_{\text{samp}}$, allowing a processing of the stored signal form with a decreased frequency. After a readout, any remaining voltage at the output buffer can be removed by closing the *Reset* switch. This picture was adopted from [28].

subsequently. For a sampling time of t_{samp} the signal charge is integrated in the first cell, before the corresponding switch S_1 is opened and S_2 is closed, to write to the next cell. In case of a readout trigger, the sampling is stopped by opening all *Write* switches. Instead, the *Read* switch is closed and the content of each cell is transmitted to the analog output one after the other in a similar manner as for the write process. The readout time t_{read} for each cell is defined by the available frequency of the following components, in general the data is

digitized right after the SCA by an ADC. With a much longer readout time $t_{\text{read}} \gg t_{\text{samp}}$, a higher effective sampling rate of the raw signal can be achieved in comparison to a direct digitization.

4.1.2 Domino Ring Sampler 4 (DRS4)

The switched capacitor array chosen for the readout of the *CEPA* crystals is the Domino Ring Sampler 4 (DRS4), which was developed by Stefan Ritt at the Paul-Scherrer Institut (PSI) in Villigen, Switzerland. It provides nine sampling channels as the one described in the previous chapter, each consisting of 1024 storage capacitors with 150 fF. This section summarizes the main features and requirements of the DRS4 as described in its datasheet [29].

Theory of Operation

The internal setup of the DRS4, depicted schematically in figure 4.3, sets specific requirements for the analog input signal. The DRS4 works with a single power supply of 2.5 V, therefore the input signals have to be positive as well. Over that, the range is restricted by the NMOS transistors, which are used as switches for the sampling capacitors. To avoid a nonlinear behavior of these transistors, the input signal should be within $0.1 - 1.5$ V. Each channel has a differential input, allowing maximum sampling voltages of 1 Vpp. Therefore, a common mode of approximately $U_{\text{CM}} = 0.9$ V of the differential input signals allows the use of the full range. The sampling frequency of the DRS4 is controlled by the so called *Domino wave*, a series of 1024 double inverters. A simplified schematic of the *Domino wave* is given in the top of figure 4.3. A low-to-high transition of the logic input DENABLE above a level of 2 V starts a pulse traversing through the 1024 double inverter blocks. The propagation speed of this pulse is defined by the time delay of the RC-circuit, formed by a NMOS transistor as voltage controlled resistor and the parasitic input capacitance of the following inverter. The resistance is controlled by the voltage applied to analog voltage input DSPEED, but depends on the power supply voltage and the temperature. Therefore, the so called DTAP logic output signal is generated by the *Domino wave*. It toggles its state after each cycle of the *Domino wave*, generating a clock of frequency $f_{\text{DTAP}} = f_{\text{DOMINO}}/2048$. This output can then be coupled via an internal Phase Locked Loop (PLL) to a differential reference clock signal, which is provided in LVDS standard to the DRS4. The *Domino wave* controls the current cell position of all nine channels simultaneously. If the logic input DWRITE is high, the traversing pulse enables the sampling of the signal to the capacitors.
For readout, the global DWRITE signal has to be lowered and the *read* signal in figure 4.3 activated. Each cell has a readout buffer, which shows a good linearity for input voltages in the range between 1.05 V and 2.05 V. Thus, the capacitor voltage during readout can be shifted up by applying a voltage to the analog input ROFS ("read offset"). The voltage seen by the readout buffer is then $U_{\text{buffer}} = U_{\text{IN+}} - U_{\text{IN-}} + U_{\text{ROFS}}$. For a differential input range of -0.5 V to $+0.5$ V a voltage of 1.55 V has to be applied to ROFS. In addition, each channel of the DRS4 has a buffer at each analog output, which shifts the output again to a range from 0.8 V to 1.8 V. Performing an offset calibration for each cell of the DRS4, a low noise of 0.35 mV and a high Signal-to-Noise-Ratio of 69 dB can be achieved.

Configuration

The DRS4 comes with a variety of possible configurations, which have to be defined during startup and readout. The interface for configuring the DRS4 consists of the logic input SRIN, the external clock SRCLK and the logic output SROUT, which are used in combination with the four address bits A3-A0. Table 4.1 lists the address bit settings, which are required for

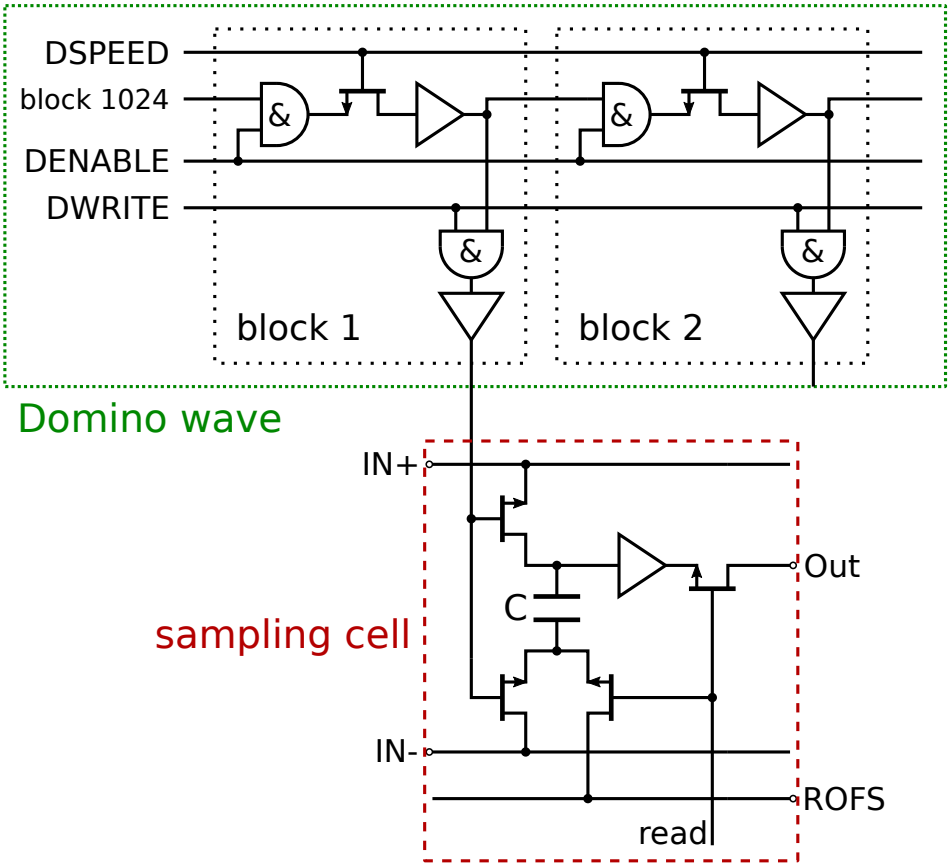


Figure 4.3: Simplified schematic of the *Domino wave* generation (green) and the sampling cells of the DRS4 (red). The rising transition of DENABLE starts a pulse, which traverses through the 1024 blocks of the *Domino wave*. An AND gate at the input of each block allows to stop the *Domino wave* at any position by lowering DENABLE. The following NMOS transistor works as voltage controlled resistor and builds a RC circuit with the parasitic input capacitance of the subsequent buffer amplifier. The characteristic rise time of this circuit determines the speed of the *Domino wave* and can be adjusted by the voltage applied to DSPEED. A second AND gate in each block of the *Domino wave* checks for the traversing pulse and the logic input DWRITE. If both signals are present, the NMOS transistors, which connect the differential inputs IN+ and IN- to the corresponding sampling capacitor C, are activated. For readout the writing has to be disabled by lowering DWRITE. A "read" signal starts the transmission of the capacitor voltage via a readout buffer to the channel output. As this buffer limits the range from 1.05 V to 2.05 V due to a nonlinear behavior, the stored voltage can be shifted by appliyng a readout offset to the ROFS pin of the DRS4. This picture was adopted from [29].

operation and a simple read out of the DRS4. The *Write Shift Register* consists of eight bits, defining the currently active channels of the DRS4. After each revolution of the *Domino wave*, the bits are shifted by one position. In this thesis, all channels are used in parallel.
The *Config Register* enables particularly the continuous operation of the *Domino wave* and the PLL. It consists also of eight bits, which are set to '1' by default, enabling the mentioned functions.
The *Read Shift Register* is required for the readout of the DRS4. As the *Domino wave* controls the consecutive activation of the capacitors during sampling, the readout is performed with the frequency given by the SRCLK input clock. A '1' in the *Read Shift Register* defines the position of the currently readout capacitor in the array. On each clock cycle of SRCLK, the position is

A3	A2	A1	A0	Output
1	0	0	1	Enable OUT0-OUT8
1	0	1	0	Enable Transparent Mode
1	0	1	1	Address Read Shift Register
1	1	0	0	Address Config Register
1	1	0	1	Address Write Shift Register

Table 4.1: Address Bit Settings of the DRS4. This table is a reduced version of the address bit settings given in [29].

shifted by one, reading out the subsequent capacitor. This register has to be configured either initially, when using the Full Readout Mode, or every time before a Region-Of-Interest (ROI) readout. These readout modes are described in the following. The three registers of the DRS4 are addressed, by applying the corresponding bit setting to the logic inputs A3-A0. On each rising edge of the SRCLK signal, the currently applied logic level at SRIN is written into the register. After a completed setup, the address bits have to be changed to configure the next register or enabling the "Transparent Mode". For the readout of all DRS4 channels, a special address bit setting has to be applied to A3-A0 (see table 4.1), generating the "read" signal described in the section before.

Readout

The switched capacitor array DRS4 enables the buffering of a signal at a high sampling frequency up to 5 Gs/s, with a decreased output rate of $10\,\text{MHz} < \text{f}_{\text{read}} < 40\,\text{MHz}$ in the case of a trigger. This readout can be done in two different modes.
In the *Full Readout* mode all 1024 cells of each channel are read out and the stored signal heights transmitted to the nine differential outputs of the DRS4. For that purpose, the DWRITE signal is lowered to stop the sampling of the input signal, while the *Domino wave* is held active. After enabling the readout of all channels by setting the address bits A3-A0 to "1001_b", the content of the first cell is transmitted to the analog output. Each clock cycle of SRCLK shifts the current read position by one, until all 1024 cells are read out. The DRS4 is designed to work with a readout frequency in the range $10\,\text{MHz} \leq f_{\text{SRCLK}} \leq 40\,\text{MHz}$. To reduce any necessary changes to the existing firmware, the readout frequency for the *CEPA* readout is set to $f_{\text{SRCLK}} = 25\,\text{MHz}$. The absolute dead time per *Full Readout* is therefore given as sum of the slow readout speed and some time for start and stop of the readout, resulting in $t_{\text{FR}} \approx 41\,\mu\text{s}$.
The dead time can be drastically reduced in the ROI mode, where only a short part of the signal has to be read out. The situation is depicted in figure 4.4. A short pulse (red) is sampled in a DRS4 channel, but the exact position is not known. In an external circuit the same pulse generates a readout trigger (black), which can be used for the determination of the interesting cell positions. For that purpose, the *Domino wave* has to be stopped after one revolution of the *Domino wave* t_{DTAP} reduced by the time window of interest before the trigger point t_1. A pulse on the RSRLOAD pin of the DRS4 pin transfers the stop position into the *Read Shift Register* and reveals the content of the corresponding cell at the output. Again, each consecutive pulse of SRCLK transfers the following cell contents to the analog output. In contrast to the *Full Readout* mode, only those cells in the region of interest are read out. With a period of the *Domino wave* of approximately $t_{\text{DTAP}} \approx 1\,\mu\text{s}$ at a sampling rate of 1 Gs/s, the dead time in the ROI mode becomes $t_{\text{ROI}} \lesssim 1\,\mu\text{s} + n \cdot 40\,\text{ns}$ when reading out n cells.

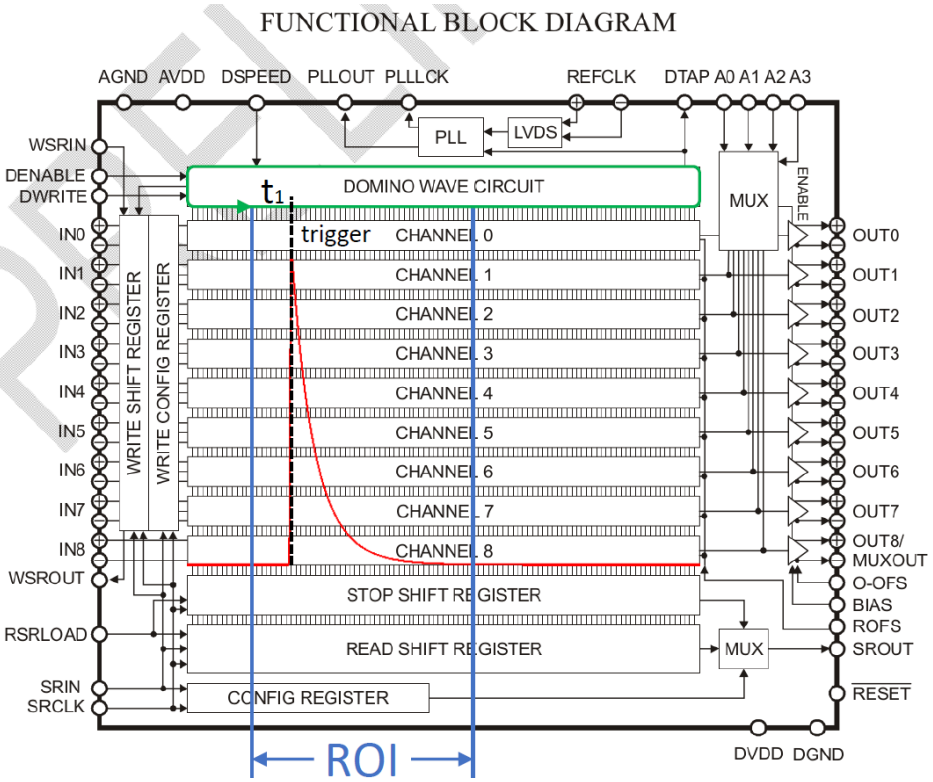


Figure 4.4: Scheme of the *Region-Of-Interest (ROI) Readout* mode, based on the DRS4 schematic block diagram from [29]. A short pulse (red) is sampled in a channel of the DRS4 and generates an external trigger (black). In order to read out only the interesting part of the waveform, the *Domino wave* has to be stopped several cell positions before overwriting the trigger point (green). A pulse on the RSRLOAD pin of the DRS4 starts the readout at this stop position, and each clock cycle of SRCLK reveals the next cell contents at the output. The length of the ROI in cell numbers defines the effective dead time of the DRS4.

4.2 Analog Preprocessing of Signals

The input signals of the DRS FEBEX Add-on Board are the raw signals from the photomultiplier tubes, which might carry high frequent perturbations or offsets. In order to improve the signal quality for the following sampling and to match the signal properties to the DRS4 input requirements, these analog inputs are preprocessed in a first step. The different corrections and transformations are described in the following.

4.2.1 Gain Stages

When a high-energy proton hits a detector unit in the *CEPA* part of *CALIFA*, the maximum deposited energy inside the scintillation crystals is about 300 MeV. According to the manufacturer [16, 17], the two materials have a light yield of 63 $\frac{\gamma s}{\mathrm{keV}}$ and 49 $\frac{\gamma s}{\mathrm{keV}}$, respectively. We approximate the quenching for protons, the quantum efficiency and light collection in the PMT with an overall duty factor of $\varepsilon \approx 10\%$. The generated photons are read out by a Hamamatsu photomultiplier tube with a quantum efficiency of about 43% in the corresponding wavelength and a typical gain of 10^6 [8]. Assuming an equal energy loss of $E = 150\,\mathrm{MeV}$ in each crystal neglecting the Bragg curve for a simple extrapolation, the output of the PMT delivers therefore a sum of $N_1 = 4.06 \cdot 10^{11}\,\mathrm{e}^-$ ($LaBr_3$) and $N_2 = 3.16 \cdot 10^{11}\,\mathrm{e}^-$ ($LaCl_3$) electrons. As stated

in 2.3, this luminescence signal is of the form

$$L(t) = \frac{N_1}{\tau_1} \cdot \exp -\frac{t}{\tau_1} + \frac{N_2}{\tau_2} \cdot \exp -\frac{t}{\tau_2}. \tag{4.1}$$

The resulting peak currents are therefore given as $N_{1,2}/\tau_{1,2}$ with values of 4.07 A ($LaBr_3$) and 1.81 A ($LaCl_3$). The PMT signal is transmitted to the DFAB via coaxial cables with a wave impedance of 50 Ω and a corresponding termination of 50 Ω on the board. Hence, the input peak voltage is approximately $U_{\max} \approx 294$ V. Such peak voltages are far outside the input range of any used component, so the input has to be attenuated for high-energy protons to fit the 1 Vpp differential input range of the DRS4, even using reduced gain at the PMTs.
Considering a well calibrated attenuation at the board input for the highest possible signals of a 300 MeV proton, the resulting DRS4 input for a γ with the lowest expected energy of 100 keV is only 0.33 mVpp. As each analog input of the DRS4 has a noise level at 1 GHz of typically 0.35 mV, the noise of the differential input will be larger than the γ signal. The implementation of different gain stages allows to use different modes depending on the current energy range of interest.
On the DFAB this is realized by a combination of two successive attenuators (see appendix A.2), which are placed very close to each other to achieve an effective 50 Ω termination for the incoming PMT signal. As the PMT produces a negative output voltage due to the generated electrons, but offsets might shift the signal also to a positive range, all components have to be driven in a dual supply mode. The chosen precision multiplexer MUX509 from Texas Instruments [30] with dual 4:1 single-ended channels is ideally suited for the selection of the currently required gain stage for two channels at once, reducing thereby the required logic wires from the FPGA on the FEBEX board.
In a recent internal study at the Chalmers University in Gothenburg ([31]), the performance of the Hamamatsu photomultiplier was investigated for high-energy events. A test dectector consisting of four $LaBr_3/LaCl_3$ phoswich combinations, was irradiated with γ-rays from a ^{60}Co-source and cocmic muons with an energy deposit up to few tens of MeV. The detectors were read out by Hamamatsu R7600U-200 photomultiplier tubes, which were supplied with high voltages between 600 V and 800 V. The PMT signal was attenuated by successive splitters and read out with a CAEN DT5730 module, which uses the DRS4 chip, and an oscilloscope. When the PMT output exceeded a voltage of $13 - 16$ V, waveform distortions were observed. A new approach, which is currently under investigation, is therefore to use a double readout of each phoswich by taking the signal from an earlier dynode for high-energy particles, such not overcoming the critical output voltage, and taking the fully amplified signal only for low-energy particles. As a result, each crystal is read out and stored in two different DRS4 channels with different gains, enabling a similar handling of the data as in the *iPhos* part of the *CALIFA* endcap.

4.2.2 Offset Correction and Decoupling

After the input signal is correctly attenuated, it has to be decoupled from the following signal processing to avoid reflections and crosstalk. The high-speed, closed loop buffer LMH6559 from Texas Instruments [32] with a fixed gain of 1 is used for that. This operational amplifier has a high full power bandwidth of 1050 MHz and a fast slew rate of 4580 $\frac{\text{V}}{\mu\text{s}}$, therefore any distortion effects on the rising and falling edges of the signal are negligible. In addition any possible offset voltage due to leakage currents of the multiplexer or other unknown effects from the PMT are filtered out by a passive high-pass filter in front of the buffer. The values of the components are chosen in a way that a very low cut-off frequency is attained. In figure 4.5 the simulated effect of the high-pass time constant $\tau = R \cdot C$ on an exemplary waveform is

shown. For small time constants, the filter capacitor discharges simultaneously to the decay of the raw signal, which results in a decreased decay time and an undershoot. The DFAB uses therefore a high/pass filter with a decay time of $\tau = 50\,\text{ms}$. However, the buffer itself causes a

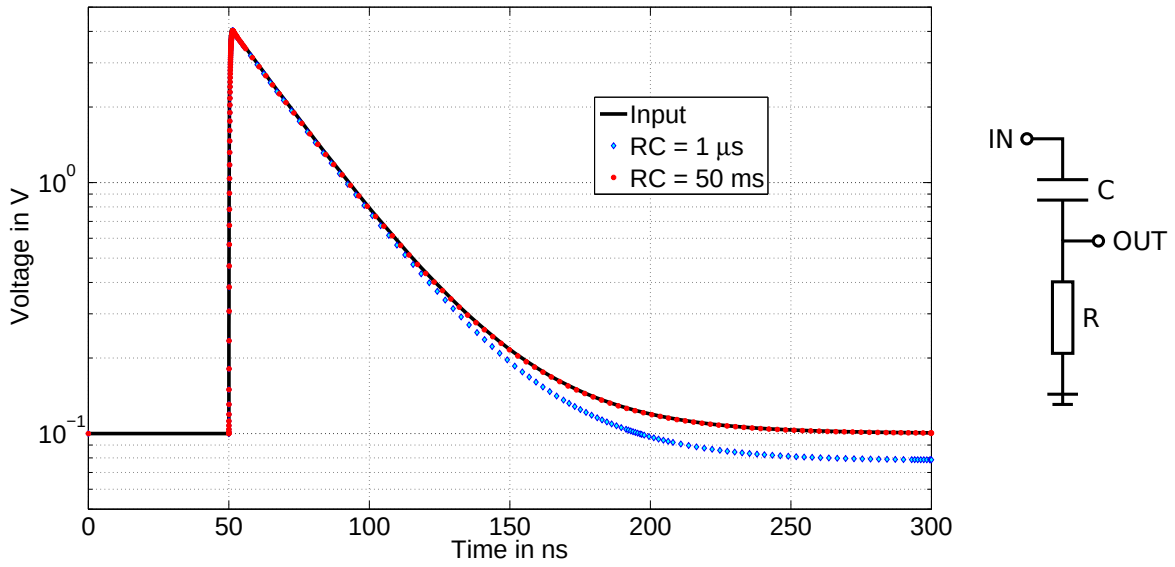


Figure 4.5: Distortion of an exponential decay after high-pass filters with different time constants $\tau = R \cdot C$. The signals are shifted up by 0.1 V to visualize the negative undershoot and the distortion of the decay time for the low time constant (blue). The simulation was performed with LTSpice.

baseline shift due to its own input bias current: Such an offset will translate into a differential signal offset after the single-ended to differential converter. As the input of the ADCs and the DRS4 have an input range of 1 Vpp, this would lead to a permanently decreased dynamic range. Therefore, the output of the buffer is AC coupled to the following signal processing.

4.2.3 Differential Signal Transmission

Signal transmission with more or less unshielded lines like on a printed circuit board can be strongly influenced by external electromagnetic fields. Dealing in the GHz frequency domain the PCB design has to be done extremely careful to avoid crosstalk and signal alterations. For example digital lines crossing low noise input signal lines might induce peaks due to the fast switching times and therefore a crosstalk in a wide frequency band. One way to reduce those effects is to use a pair of strip lines, which are positioned close to each other and carry the mirrored waveform of each other. The differential voltage of this pair describes the original signal shape, most effects are apllied to both lines in the same way and cancel each other. The geometric properties of the differential pair defines the wave impedance and has to be controlled to avoid reflections (see appendix A.1).
On the DFAB, the decoupled single-ended output signal from the LMH6559 has to be converted into a differential signal. This is done using the high speed differential amplifier ADA4932 from Analog Devices [33] in a symmetric amplifier circuit, as depicted in figure 4.9. The feedback resistors are chosen for a gain of 1, so the differential lines have half the input amplitude and are mirrored to each other. Therefore, the amplifier ADA4932 is driven with a dual power supply of $V_s = \pm 5\,\text{V}$.
According to the Nyquist-Shannon theorem, no higher frequencies than the Nyquist frequency

of half the sampling frequency can be reconstructed from the digitized waveform correctly. Any higher frequencies will be misinterpreted and introduce errors. To avoid this effect, the analog input signal has to be filtered with a cutoff frequency of about $f_{\text{cutoff}} \approx 500\,\text{MHz}$. A common approach is to use a high-order low-pass filter, when converting the single-ended signal into a differential one. In the first revision of the DFAB this approach was realized. With a desired cutoff-frequency of $f_{3\text{dB}} = 500\,\text{MHz}$, the resulting capacitor of the values are in the order of some pF, thus comparable to the parasitic properties of the amplifier. Beyond that, the complex setup of the filter requires additional space and ground connections on the add-on board. A alternative approach utilizing the internal transfer function of the ADA4932 was therefore studied. With a cutoff-frequency of 560 MHz ([33]) for a gain of 1, the ADA4932 limits the transmitted frequencies to the desired bandwidth. A simulation in LTSpice compared the transfer functions in dependence of the frequency for circuits with a second order Besselfilter and a simple amplifier and is depicted in figure 4.6. The setup using a Besselfilter (blue) shows a lowered cutoff frequency of about $f_{3dB,Bessel} \approx 250\,\text{MHz}$, whereas a setup without additional filter has a cutoff frequency in the desired range of $f_{3dB} \approx 490\,\text{MHz}$ as well as a steeper clipping. After converting the single-ended signal into a differential one, it

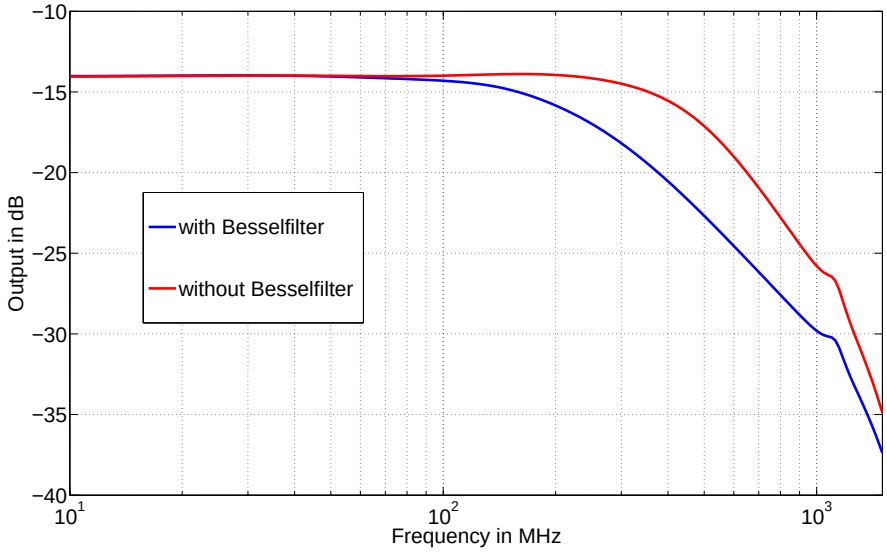


Figure 4.6: Transfer functions in dependence of the frequency for an amplifier circuit using the ADA4932 in a LTSpice simulation. A second order Besselfilter (blue) in the amplifier circuit gives a cutoff-frequency of about $f_{3dB,Bessel} \approx 250\,\text{MHz}$, although the component values are chosen for a cutoff at 500 MHz. In contrary using a simple amplifier circuit with gain 1 shows the expected behavior of the ADA4932 with a cutoff-frequency of $f_{3dB} \approx 490\,\text{MHz}$.

is directly transferred to the DRS4. The analog input pins of the DRS4 require positive signals in the range of $0.1 - 1.5\,\text{V}$ as mentioned before. For a differential signal this means a common mode has to be added. A first approach used the built-in common-mode pin of the ADA4932, which adds the adjacent voltage to the output. Simulated signal curves are depicted in the left of figure 4.7. The common-mode voltage is not only added to the outgoing differential pair, but also interacts with the input of the differential amplifier via the feedback path. As a result, the differential signal is shifted by a remarkable offset, which constrains part of the available 1 Vpp input range of the DRS4. The best solution to overcome this effect is an AC coupling after the differential amplifier and adding the common-mode with a passive circuit, as it is done on the DRS4 evaluation board from PSI. A common-mode of 1 V is applied to the

two differential lines via a small inductance, so that the DC common-mode sees no resistance and is added to the signal, while the fast signal pulses are not affected. This additional circuit was positioned in the second revision of the DFAB as close to the DRS4 inputs as possible to avoid reflections due to a wrongly terminated transmission line (compare appendix A.1).

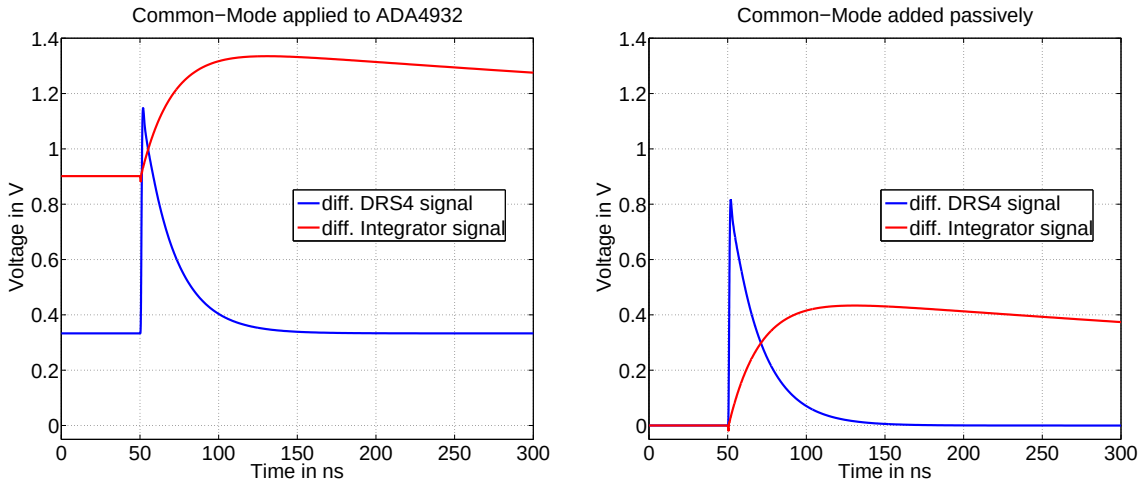


Figure 4.7: Offset generation when applying the common-mode of $v_{\mathrm{CM}} = 1\,\mathrm{V}$ to the common-mode pin of the differential amplifier ADA4932 (left). The interaction of input and output of the amplifier via the feedback path induces an offset of the differential signals. When the common-mode pin is connected to ground and 1 V is added passively to the differential signal after an AC coupling (right), no such offset is generated.

4.2.4 Integrator

As discussed in section 4.1.2 the DRS4 is an analogue chip externally triggered without anty internal trigger capability. To provide a free running mode which is cenceptually foreseen in the *CALIFA* calorimeter an additional trigger branch was implemented in the DFAB. The decoupled output signal of the LMH6559 buffer is not only fed to the DRS4, but split into a trigger branch for an independent trigger generation on the FEBEX board. When the raw signal at this stage is transmitted directly to the FEBEX board, the same challenges as described in section 3.2 would occur. Especially the comparatively slow sampling misses a major part of the waveform, thus the amplitude measured in the first signal sample may have already decreased below the trigger threshold and low energy events are not detected reliably. Hence, the raw signal is integrated on the DFAB reducing the noise and "stretching" the pulse to be sampled and analysed on the FEBEX board with the existing readout algorithms. Again, the differential amplifier ADA4932 is used in an integrator circuit with a decay time constant of $\tau = 1\,\mu\mathrm{s}$. This time is chosen to guarantee a good representation of the deposited energy in the crystals ($\tau \gg \tau_{\mathrm{LaCl3}}$), but avoiding pile-up due to a long signal tail. By this method a signal shape similar to the preamplifier signals for the *Barrel*-part of *CALIFA* (see figure 3.4 and 4.7) is generated which can be treated with identical algorithms as described for the CsI(Tl) part of the detector, just adjusting the different time constants. With this method not only a low threshold trigger is generated, but also the total energy deposit could be evaluated.

4.3 DRS4 FEBEX Add-on Board (DFAB)

In the framework of this master thesis a first prototype of the DRS4 FEBEX Add-on Board (DFAB), depicted in figure 4.8, was designed and produced. This prototype already included all the features as described before and was already operated together with the FEBEX 3B mother board. It processes eight channels in parallel, which are sampled and buffered in one

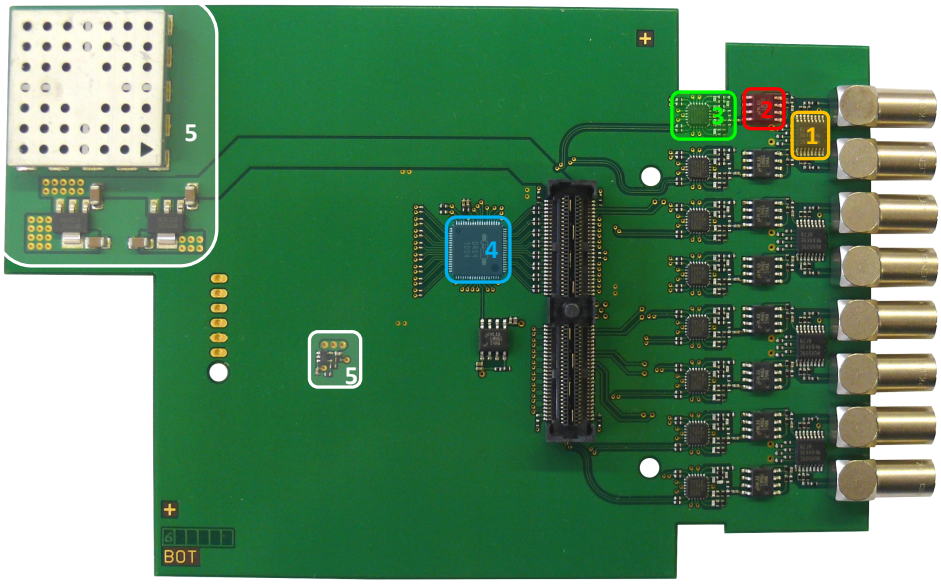


Figure 4.8: First revision of a DRS4 FEBEX Add-on Board (DFAB) prototype. (1) MUX509 switches the current gain stage of the input signal (2) LMH6559 buffer decouples the raw input waveform from the following preprocessing (3) ADA4932-2 differential amplifier, housing two independent amplifiers for integration and single-ended to differential conversion (4) DRS4 chip, sampling the waveform with approximately 1 Gs/s. For a readout the output is directly transmitted to the ADCs on the FEBEX board. (5) The supply voltages of $V_s = \pm 5$ V, $V_{\mathrm{DRS4}} = 2.5$ V and $V_{\mathrm{CM}} = 1$ V are generated on the board, as far from the signal lines and processing as possible. The step-down regulator LTM8023 is surrounded by a cage for additional shielding.

DRS4 chip. The input signals are connected to the DFAB via eight LEMO connectors and terminated in a combination of resistive voltage dividers. Four MUX509 multiplexers (1) are used to switch the currently used gain stage of two channels each. The individual signal is then decoupled from the following preprocessing by eight LMH6559 buffers (2), before it is split up into two branches and processed by the ADA4932 differential amplifiers (3). In one branch, the signal is integrated and send differentially to the FEBEX board for trigger generation. In the other branch the signal is converted from single-ended to differential and transferred into the DRS4 chip (4), which samples at approximately 1 Gs/s. For readout the output of the DRS4 is transmitted to the FEBEX ADCs. A simplified circuit diagram of the whole preprocessing is depicted in figure 4.9, the detailed schematic of one channel can be found in appendix B. The linear regulators for generating the required supply voltages (5) are positioned as far from the signal processing as possible to avoid any crosstalk or perturbations. To avoid signal alterations and reflections (see appendix A.2), the whole preprocessing is positioned compact and close to the input connectors, so that the signal can be transmitted differentially on the board. For a well defined wave impedance of the differential pairs, the corresponding layer is shielded by two surrounding ground layers. In addition, two separate layers are required for the

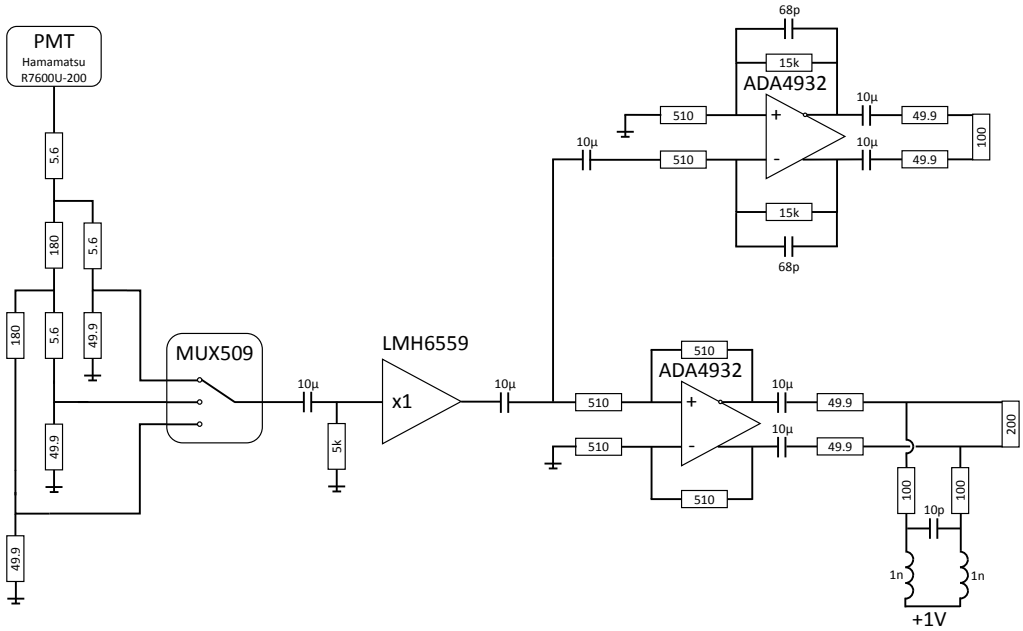


Figure 4.9: Simplified circuit diagram of the DFAB preprocessing.

distribution of the different supply voltages. The layer facing the FEBEX board is equipped with the electronic components. Thus, the DFAB is build on a six layer circuit board, which was produced by Multi Circuit Boards Ltd.[3]. The detailed layer structure is specified in table 4.2. The permittivity of the used insulator FR4 is stated by Multi Circuit Boards Ltd. to be

Nr	copper	insulator FR4	purpose
1	35 μm		GND layer, power capacitors
		156 μm	
2	35 μm		GND layer, differential signals
		200 μm	
3	35 μm		GND layer
		360 μm	
4	35 μm		power supply
		200 μm	
5	35 μm		GND layer, CM distribution
		156 μm	
6	35 μm		GND layer, preprocessing

Table 4.2: Layer composition of the DRS4 FEBEX Add-on Board.

$\varepsilon_r = 4.6$ at 1MHz [34]. This was used to calculate the properties of the differential lines for well defined wave impedances with the free Saturn PCB Design Toolkit[4]. The layer carrying the differential signals sits asymmetrically between two ground layers with a distance of 156 μm and 200 μm respectively. The chosen properties of these edge coupled internal asymmetric differential pairs are a width of $d_{\text{wire}} = 5$ mil with a spacing of $d_{\text{space}} = 10$ mil, resulting in a wave impedance of $Z = 97.4\,\Omega$. While this ensures minimum reflections of the differential signals, due to the alternating alignment of integrated signals and DRS4 signals, it is not

[3]https://www.multi-circuit-boards.eu/en/index.html
[4]https://www.saturnpcb.com/pcb_toolkit.htm

possible to use only one layer for them. The intergated signals, which are used primarily for trigger generation and therefore tolerate more noise, are therefore wired on the bottom layer to cross the DRS4 signals. To avoid again any reflections at the transition from the bottom layer to the differential layer, the wave impedance of the edge coupled external differential pairs has to be adjusted as well. A wire width of $d_{\text{wire}} = 6\,\text{mil}$ with a spacing of $d_{\text{space}} = 10\,\text{mil}$ provided a wave impedance of $Z = 100.9\,\Omega$ here. A discussion of the wave impedance and its effect on reflections can be found in appendix A.1.
The DFAB is connected to the FEBEX board via a 104-pole Samtec connector. It provides 16 differential pairs to the FEBEX ADCs and 16 differential or 32 single-ended connections, respectively, to the FPGA. Four of those connections are reserved for special inputs, leaving 28 connections for the DFAB configuration. Eight lines are used for the adjustment of the gain stages, 14 for the control of the DRS4. A detailed overview of the connections between the DFAB and the FEBEX FPGA can be found in appendix B.1 in table B.1.

4.4 Power Supply

The FEBEX board provides only a power supply of +12 V to the add-on board. The components of the DFAB however require supply voltages of $V_s = \pm 5\,\text{V}$, $V_{\text{DRS4}} = 2.5\,\text{V}$ and $V_{\text{CM}} = 1\,\text{V}$. Linear regulators (REG1117-5, REG1117A-2.5 and ZXRE060H5) are used for the positive supply voltages to minimize the noise. The negative supply voltage of $V_s = -5\,\text{V}$ is generated with the DC/DC Step-Down μModule Regulator LTM8023 [35], which is used on the FAB also. In the first revision of the DFAB the regulator setup was therefore adopted from the FAB, only the component values were changed according to the datasheet [35] in order to produce a voltage of $-5\,\text{V}$. Due to the higher power consumption of the DFAB during startup, the LTM8023 output voltage broke down before a stable negative voltage could be assembled. In contrary to the FAB, an additional "soft start" has to be implemented for the DFAB: a RC-filter at the RUN/SS limits the maximum input current during the start-up. This method was tested on an evaluation board and worked extremely stable. As the LTM8023 comes in a Land Grid Array (LGA) package, the pins were not accessible after the assembly of DFAB revision 1.0. Therefore, the soft start will be implemented in the next revision only. For basic tests (see section 5), the negative supply voltage was generated in an external power supply.

4.5 FEBEX 3B Firmware changes

A firmware for the control and calibration of the DRS4 chip will be developed in the master thesis of Giovanni Bruni at the Chalmers University in Gothenburg, Sweden. However, for basic tests of the DFAB the existing CsI readout firmware described in section 3.1.2 was extended by an entity for a simple readout of the DRS4 and a Phase Locked Loop (PLL) for the generation of the reference clock with $f_{\text{REFCLK}} = 500\,\text{kHz}$. The firmware is written in the ***V**ery High Speed Integrated Circuit **H**ardware **D**escription **L**anguage* (VHDL) and works with an internal 100 MHz clock. A major change had to be applied to the ADC sampling, as the DRS4 requires a specific delay between its output and the ADC sampling. The timing scheme of the DRS4 readout is depicted in figure 4.10. For best linearity, the DRS4 output should be digitized in an ADC with a time delay of $t_{\text{SAMP}} - 2\,\text{ns} = 38\,\text{ns}$ relative to the SRCLK signal, so the stored voltage can settle at the output pin. Therefore, the ADC clock and the SRCLK are generated in the new DRS4 control entity with a frequency of 25 MHz. The time delay is given by a fast clock cycle, so $\Delta t = 30\,\text{ns}$ instead of 38 ns, which reduces the linearity but enables a simple test of the DRS4 functionality without the implementation of complex Delay Locked Loops.

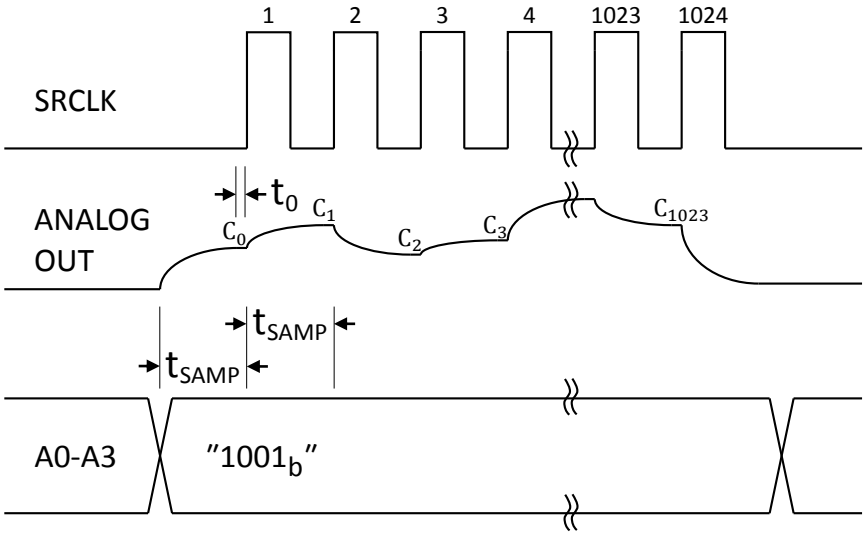


Figure 4.10: DRS4 readout procedure. The transition of the logic input bit A0-A3 to "1001_b" enables the ouput of all channels, so that the content of cell 0 is transferred to the output pin. Each consecutive cycle of SRCLK reveals the next cell content, so 1023 clock cycles have to be applied to read out all cells and a 1024th wraps the read shift register around to the first position. For best linearity the output should be digitized in an ADC about $t_0 = 2$ ns before the next rising edge of SRCLK. The scheme was adopted from [29].

The DRS4 behavior is controlled by a simple Finite State Machine (FSM). For every rising edge of the 100 MHz clock, the signal configuration is applied according to the currently set state. A change of internal signals or a counter can change the state, which becomes active at the following clock cycle.
During startup of the FPGA, the DRS4 control entity waits for 2046 clock cycles for stable clocks and supply voltages. After that, the registers of the DRS4 are configured as described in section 4.1.2: the *Config Register* enables the internal DRS4 PLL and continuous cycling of the *Domino wave*, the *Read Shift Register* sets the first cell positrion for readout and the *Write Shift Register* enables all channels for sampling. A short intermediate state of 100 clock cycles allows the settling of the new configuration before the *Domino wave* and the writing to the sampling cells is activated. In the following idle state the DRS4 runs continuously and samples the applied signals until a readout trigger occurs and stops the writing, while the *Domino wave* traverses on. For a *Full Readout* the *Read Shift Register* is configured again to ensure the same start position for every readout, before all 1024 cells of each channel are read out consecutively. After the last cell was read out, the state returns to the idle state, where the sampling is reactivated.
The VHDL code of this DRS4 control entity can be found in appendix C. For a first test of the DRS4 chip the firmware was installed on a FEBEX 3B board and tested together with a DFAB prototype. Unfortunately, we were not able to run the PLL successfully. The DTAP signal did not start to toggle its state with the reference frequency and the DSPEED voltage, controlling the speed of the *Domino wave*, decreased to GND instead of adjusting to a constant value. Applying an external voltage to the DSPEED pin without using the PLL enabled a stable DTAP signal, indicating a constant speed of the *Domino wave*. While in the transparent mode a sinusoidal test signal could be measured at the DRS4 output using the FEBEX 3B board, the output of the DRS4 stayed constant during a readout of the DRS4.
This can be caused by several sources: The *Domino wave* may not switch the active sampling

cell, so that no data is written to the sampling cells except the first one. Another possibility is that the *Read Shift Register* is not configured correctly or the rising edges of the SRCLK are too slow, so the DRS4 can not detect them and the configuration as well as the readout stays in an undefined state.
In the limited time of this master thesis it was not possible to clarify this behavior of the DRS4 chip, but adjustments of the firmware and further detailed tests will be performed in the future.

Chapter 5

Laboratory Tests

Simple tests were performed to characterize the performance of the DFAB. The tested device was a DFAB prototype revision 1.0 (schematic of one channel in appendix B) with the additional changes described in the previous chapter: Due to the break down of the step-down regulator LTM8023, the $V_s = -5\,\mathrm{V}$ supply voltage for the DFAB was generated in an external power supply. Beyond that, the Bessel filter of the single-ended to differential converter circuit was replaced by a simple amplifier circuit with gain 1. The common-mode of the differential signal was no longer applied to the ADA4932 itself, but added passively after an AC coupling of the amplifier output. In the same way a capacitor was added in between the buffer and the two signal branches to introduce an AC coupling and decouple the individual offsets caused by leakage currents.
During the test phase, there was no $LaBr_3$(Ce) detector available, so test signals similar to the known scintillation signals had to be produced. This was done by a 100 Hz TTL clock, which was processed in several logic modules and gate generators, to get a long rectangular pulse with fast rising and falling edges. The typical exponential decay of the scintillation light can then be simulated by a capacitor C in series, which discharges over the $R_{\mathrm{IN}} = 50\,\Omega$ input termination of the DFAB, resulting in a decay time of $\tau = R_{\mathrm{IN}} \cdot C$. The rectangular pulse is therefore transformed into a positive pulse at the rising edge and a negative pulse at the falling edge. A pile-up effect of those two exponentially decaying pulses was avoided by a sufficiently long rectangular pulse. The chosen capacitor values of $C_1 = 470\,\mathrm{pF}$ and $C_2 = 220\,\mathrm{pF}$ give decay times of $\tau_1 = 23.5\,\mathrm{ns}$ (similar to τ_{LaCl3}) and $\tau_2 = 11\,\mathrm{ns}$ (similar to τ_{LaCl3}).
In a first test the analog preprocessing of the DRS4 branch was studied by measuring the incoming signals at the DRS4 input pads. A Tektronix TDS 3054 C oscilloscope with a differential probe (Tektronix P6247) was used to record the signals. The measured waveforms for a fast (blue) and a slow test signal (red) are depicted in figure 5.1. A rise time of about $\tau_{\mathrm{rise}} \approx 5\,\mathrm{ns}$ can be observed for both test signals. It is created by the combination of the serial resistance of the differential lines and the parasitic capacitance of the probe input and additional wiring at the DRS4 input pads. An exponential fit of the falling slopes reveals decay times of $\tau_{1\mathrm{exp}} = 11.2\,\mathrm{ns}$ and $\tau_{2\mathrm{exp}} = 27.1\,\mathrm{ns}$. The difference to the expected theoretical values is caused by the component tolerances. Slightly changed decay times of the real $LaBr_3$(Ce) and $LaCl_3$(Ce) signals can be calibrated and taken into account in the analysis firmware. A good separation of the two test signals is possible due to the clear difference in the falling slopes. The DRS4 could not be tested yet in this masterthesis, but will be studied as part of a planned beam test at the Bronowice Cyclotron Center in Krakow in summer 2017.
The integrator branch of the DFAB was tested using the firmware described in section 4.5, which uses the existing trigger generation and waveform analysis firmware of the CsI(Tl) readout. The only change concerning the integrator signals is the decreased sampling speed $f_{\mathrm{ADC}} = 25\,\mathrm{MHz}$ of the ADCs on the FEBEX board due to the DRS4 readout procedure (see

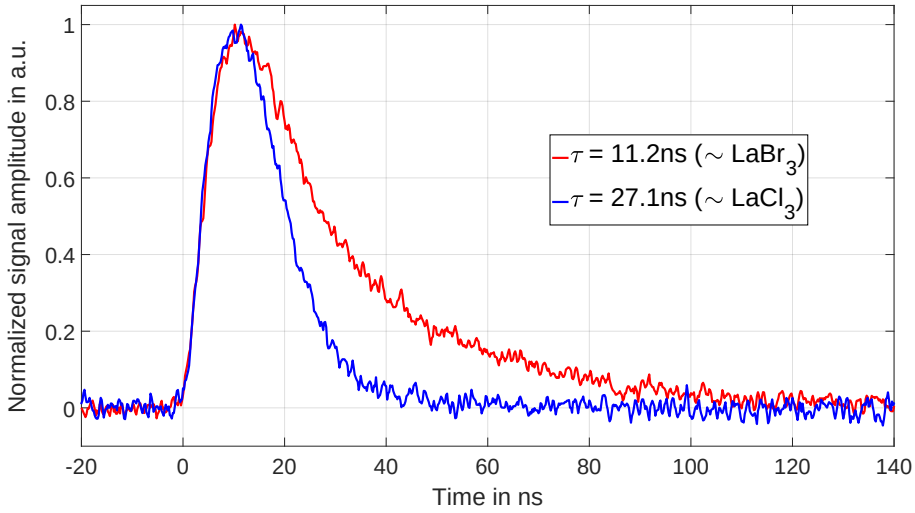


Figure 5.1: Preprocessed signals at the DRS4 inputs with fast ($\tau = 11.2$ ns, blue) and slow ($\tau = 27.1$ ns, red) exemplary decay times. The rising edges of the signals are defined by the bandwidth of the ADA4932 amplifier and the additional capacitive load due to the measuring probe. The different decay times allow a clear separation of the two test signals.

section 4.5). The integrator signals are primarily used for the readout trigger generation, but also allow for a validation of the reconstructed total energy deposit in the scintillation crystals. Therefore, the resolution of the integrator branch is of special interest and was studied by measuring the signal maximum after the MWD of the fast test signal described before. The MWD window size was set to 20 samples (800 ns length), and the integrator decay time in the MWD set to $\tau_{\mathrm{MWD}} = 1200$ ns. The decay time is chosen higher than the real one given by the integrator circuit, so that the reconstructed MWD signal has a clear maximum before it is cut off by the MWD window size. Otherwise, the signal increases monotonously in the MWD window and the maximum value is determined by the window size instead of the reconstructed pulse height. The resulting distribution of the measured signal height in terms of sampling channels is shown in the histogram in figure 5.2. Assuming identical input signals, the integrator resolution is determined by its noise and therefore a Gaussian distribution is expected. The observed distribution of the reconstructed signal heights however differs strongly from the expectation. It can be explained by a varying time position of the integrated signal in comparison to the discrete sampling times. The underlying effect is illustrated in figure 5.3. Two exemplary integrator signals are shifted in time to have a delay of 37 ns (green) and 3 ns (blue), respectively, in comparison to the fixed sampling in the ADC (black vertical lines). For both signals the trigger threshold (red line) is exceeded for the sampling at $t = 0$, but the following samples of the blue curve are commonly shifted up in comparison to the green samples. Thus, the MWD algorithm will reconstruct a higher maximum height of the blue curve than for the green one. While the time shifts of the real signals are expected to be random, the reconstructed maximum depends on the wave form and is no longer equally-distributed. The observed distribution in figure 5.2 is therefore the convolution of this sampling-induced effect and a Gauss distribution due to the integrator noise.
As the measured waveforms are monotonously increasing before the first signal sample exceeds the trigger threshold, the described time shift can be approximated in first order by the amplitude of this first signal sample. In figure 5.4 (a), this is plotted versus the reconstructed energy after the MWD for all measured traces. A clear correlation between time shift and

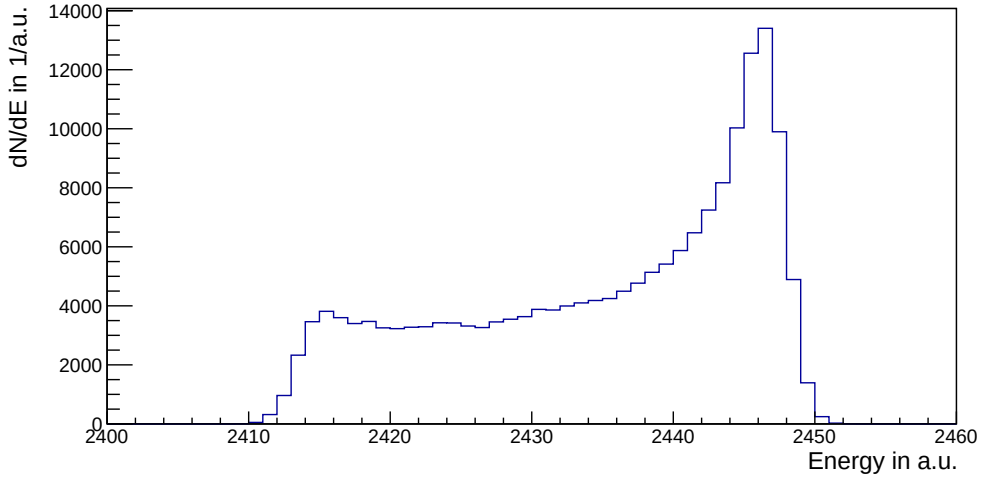


Figure 5.2: Histogram of the reconstructed energy after the MWD. For identical input signals a Gaussian distribution due to the integrator noise is expected. The present shape however is caused by a time dependance of the sampling positions along the signal waveform.

reconstructed energy of the integrated signals can be observed. The correlation curve depends strongly on the full energy deposit and the ratio of the fast and slow components N_1 and N_2. Therefore, a correction of the measured integrator energy is not directly possible. Instead, the effect of the time shift can be reduced by two simple approaches. Firstly, a longer decay time of the integrator reduces the drop of the signal amplitude between two sampling points, thus decreasing the difference in sampling between signals with different time shifts. In figure 5.4 (b) the integrator decay time was increased by a factor of 3.4 by exchanging the feedback resistors in the integrator circuits. The range of the reconstructed energies is reduced and the correlation curve becomes flatter. Secondly, an additional higher sampling rate reduces directly the possible time shift. In the existing FAB readout firmware the ADCs are digitizing the analog signals with a frequency of 50 MHz. As the integrator branch does not need to be controlled by the DRS4 entity, a test run with the CsI(Tl) firmware installed on the FEBEX FPGA could be performed. The distribution of the reconstructed energy is plotted against the amplitude of the first signal sample in figure 5.4 (c). In this case, the variation of the energy is mainly given by the integrator resolution itself. The histogram of the measurement is shown in figure 5.5. A longer decay time of the integrator in combination with a faster sampling rate reduced the time shift effect so far that the integrator resolution can be determined from a Gaussian fit to the histogram. The resulting resolution (FWHM) is approximately $\frac{\Delta E}{E}\big|_{\mathrm{FWHM}} \approx 0.14\%$ and fulfills perfectly the requirements for the CEPA. In order to use the excellent resolution of the integrator branch on the DFAB, the decay time of the integrator will be adjusted in the next revision and the firmware will be adapted to enable a 50 MHz sampling of the ADC. This is possible due to the fact, that the integrated signals of all eight input channels of the DFAB are digitized in one FEBEX ADC, while the DRS4 signals, requiring a 25 MHz sampling, are processed in the other ADC. Two separate clocks for the ADCs will allow therefore a faster sampling of the integrator signals together with an optimum readout of the DRS4. An even better timing can be achieved with the FEBEX 4 board as it is equipped with two fast sampling ADCs with a rate up to 100 MHz. While the available space on the Lattice FPGA on the FEBEX 3B board limited so far the sampling speed of the analog signals and even required a decimation of the digitized signal (see section 3.1.2), the QPID can be removed for the integrated signals as only the reconstructed energy is

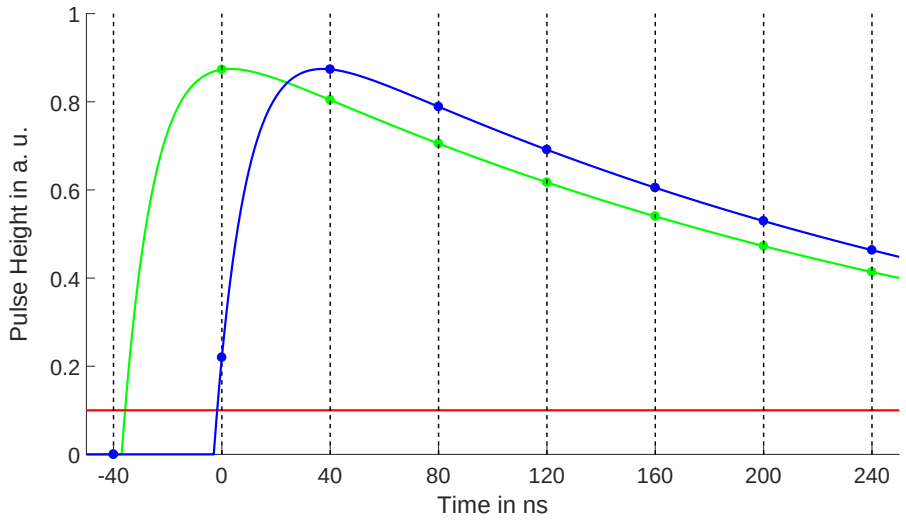
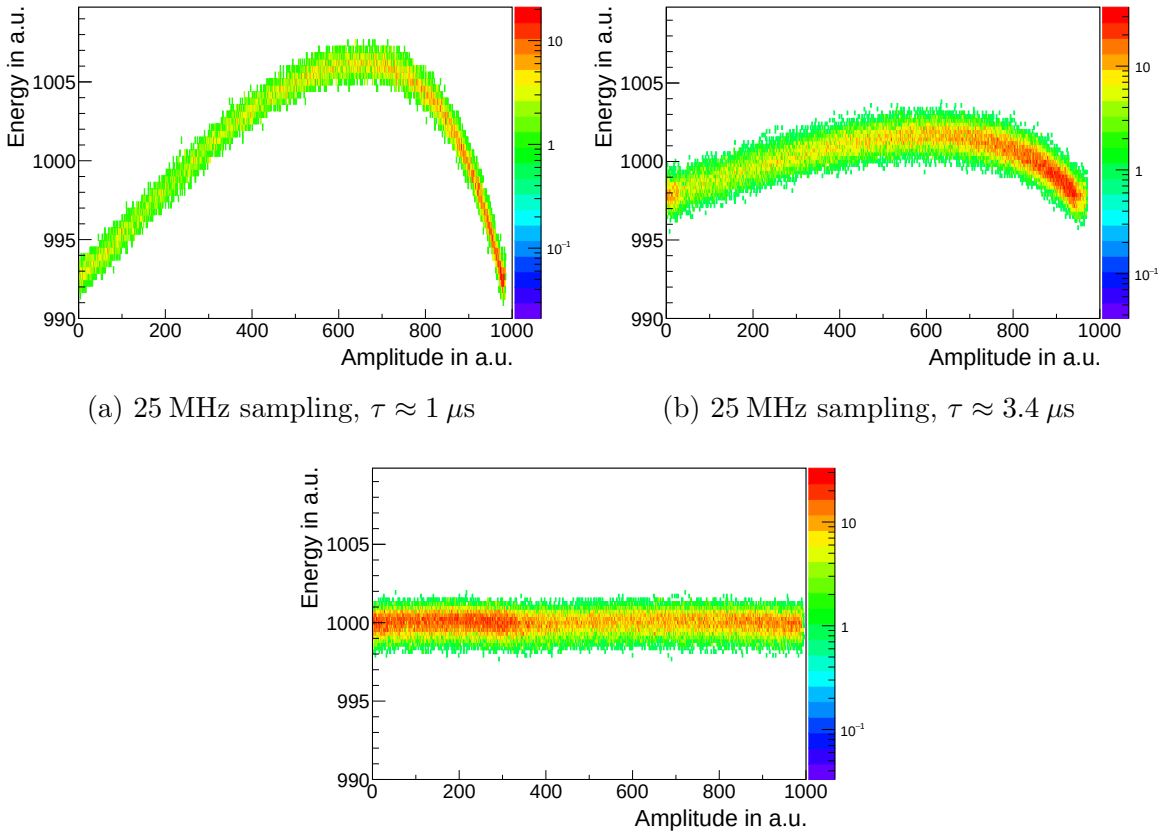


Figure 5.3: Sampling of time shifted signals. The two curves represent an integrator signal with a time shift of 37 ns (green) and 3 ns (blue), respectively. The sampled values of both signals exceed the trigger (red line) at the same sampling point $t = 0$, but the blue waveform will result in higher sample values. This difference causes a shift of the reconstructed energy after the MWD. For better illustration, a decay time of $\tau = 300$ns was used for these exemplary signals.

of interest. The scintillation components N_1 and N_2 can be calculated from the DRS4 signals and verified by the absolute energy deposit determined in the integrator branch. Any uncertainty concerning the fast component N_1, due to a decreased rise time of the DRS4 signal for example, can therefore be reduced.



(a) 25 MHz sampling, $\tau \approx 1\ \mu$s

(b) 25 MHz sampling, $\tau \approx 3.4\ \mu$s

(c) 50 MHz sampling, $\tau \approx 3.4\ \mu$s

Figure 5.4: Correlation plots of the reconstructed energy after the MWD and the amplitude of the first sample exceeding the trigger threshold for the integrator branch of the DFAB. For the initial configuration of the DFAB revision 1.0 (a) with an integrator decay time of approximately $\tau = 1\ \mu$s and a 25 MHz sampling rate of the ADC, the time position of the pulse relative to the sampling points ($\sim$ Amplitude) causes a wide variance of the reconstructed energy. By increasing the decay time to approximately $\tau = 3.4\ \mu$s (b), the extent of the correlation curve is decreased to half the previous variance. An additional faster sampling with 50 MHz (c) reduces the time dependence of the reconstruction so far, that the distribution of the reconstructed energies is dominated by the quality of the integrator signal itself. For better illustration, the data of the three measurements was normalized to share a common mean value and allow a simple comparison of the resolution given by the spread in the y-axis.

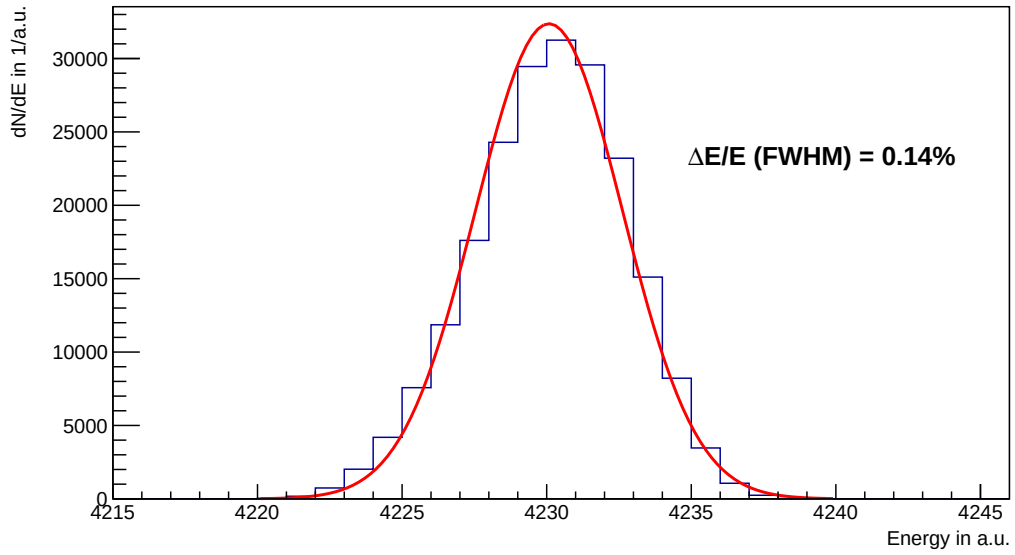


Figure 5.5: Histogram of the reconstructed energy using an integrator decay time of $\tau \approx 3.4\mu$s and a sampling frequency of $f_{\mathrm{ADC}} = 50\,\mathrm{MHz}$. A normal distribution with a slightly extended left shoulder due to sampling effect is observed. The Gaussian fit (red) determines an energy resolution of $\frac{\Delta E}{E} \approx 0.14\%$ (FWHM).

Chapter 6

Summary and Outlook

In the framework of this thesis a GHz sampling add-on board for the analysis of fast scintillation signals in the *CALIFA Endcap Phoswich Array* was developed. It is designed as an expansion to the FEBEX 3B board, to guarantee a maximum overlap with the existing readout hardware and software. The incoming analog signals from a photomultiplier tube are therefore preprocessed by the developed DRS FEBEX Add-on Board (DFAB) and analysed in the Lattice FPGA on the FEBEX 3B board. A first prototype of the DFAB was produced, which processes eight independent channels. The input can be attenuated by three different gain stages to use the full resolution of the electronics in different input ranges. Each signal is decoupled from the input and split into a sampling branch which stores the analog signals in the Domino Ring Sampler 4 (DRS4) from PSI[5] with a sampling frequency of $f_{\mathrm{DRS4}} = 1\,\mathrm{GHz}$ and an integrator branch for readout trigger generation and total energy measurements. Due to the high-frequency analog input signals the electronic components were chosen carefully to avoid signal distortions and a well defined differential signal transmission was implemented. For test purposes, exponentially decaying pulses, representing the luminescence signals of $LaBr_3(Ce)$ and $LaCl_3(Ce)$, were applied to the DFAB. To optimize the performance a Besselfilter in the DRS4 branch was exchanged with a simple amplifier circuit with gain 1 and the common-mode, required for the input of the DRS4, was added passively after a AC coupling of the signals after the single-ended to differential converter. The measured waveforms at the DRS4 pads showed a decaying slope consistent with the input signals. The rising edges of the signals were slightly flattened due to the parasitic capacitive load of the measuring probe. For the integrator branch an energy resolution of $\frac{\Delta E}{E} \approx 0.14\%$ (FWHM) was achieved by increasing the decay time of the integrator and digitizing the signal at the maximum frequency of $f_{\mathrm{ADC}} = 50\,\mathrm{MHz}$. The development of a basic firmware for the control of the DRS4 for test purposes could not be concluded in the limited time of this thesis, but will be subject of the ongoing work.
In a further step revision 2.0 of the DFAB will implement the mentioned changes as well as a soft start circuit for the linear regulator generating the negative supply voltage $V_s + -5\,\mathrm{V}$. The component values of the integrator branch will be optimized to cover the same range of incoming signals that can be processed by the DRS4. Another approach to be studied foresees to process only four crystal pairs with one DFAB, but use the signal from the last two dynodes of each photomultiplier tube to sample each channels simultaneously with two different gain stages, avoiding distortions of the waveforms for high-energy events. A test of the whole DFAB and especially of the DRS4 with the final DFAB firmware currently developed by G. Bruni[6] in his master thesis can be performed in summer 2017 at the Bronowice Cyclotron Center in Krakow with up to 230 MeV protons accelerated towards various targets.

[5] Paul-Scherrer-Institute, Villigen, Switzerland, http://www.psi.ch
[6] Giovanni Bruni, Chalmers University, Gothenburg

Appendix A

Signal Transmission

A.1 Transmission Line

The transmission of signals along physical wires requires consideration of parasitic properties of the wires themselves such as resistivity, capacitance and inductance. A simple derivation of the behavior of a transmission line is described in this section, based on the lecture slides from [36].
The assumption of a lossless transmission eliminates the resistivity, and the simple model of two symmetric wires depicted in figure A.1 can be used.

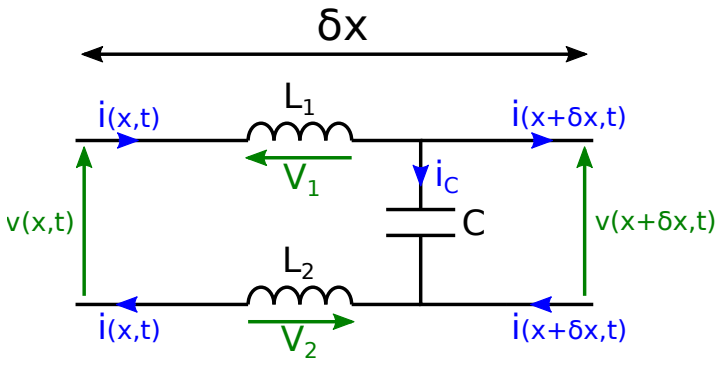


Figure A.1: Model of a lossless transmission line. The two wires carrying the signal are afflicted with a parasitic inductances L_1 and L_2 in series and a parasitic capacitance C in parallel per length δx. The picture is taken from [36].

The effect of parasitic inductances L_1, L_2 and a parasitic capacitance C is studied for a infinitesimal line length δx. According to Kirchhoff's current law, the sum of all currents in a single point has to be zero, describing the change of the current as

$$i(x,t) = i_C + i(x+\delta x, t). \tag{A.1}$$

The channge of the voltage is derived from Kirchhoff's voltage law, stating the sum of all voltages in a closed loop have to cancel:

$$v(x,t) = V_2 + v(x+\delta x, t) + V_1 \tag{A.2}$$

Due to the small spatial dimension, the change of time derivatives of the physical quantities

voltage $v(x,t)$ and current $i(x,t)$ over the length δx can be neglected:

$$\frac{\partial v(x,t)}{\partial t} \approx \frac{\partial v(x+\delta x,t)}{\partial t} \equiv \frac{\partial v}{\partial t} \tag{A.3}$$

$$\frac{\partial i(x,t)}{\partial t} \approx \frac{\partial i(x+\delta x,t)}{\partial t} \equiv \frac{\partial i}{\partial t} \tag{A.4}$$

This results in the characteristic equations for the capacitor and the inductors:

$$C \cdot \frac{\partial v}{\partial t} = i_C = i(x,t) - i(x+\delta x,t) = -\frac{\partial i}{\partial x} \cdot \delta x \tag{A.5}$$

$$(L_1 + L_2) \cdot \frac{\partial i}{\partial t} = V_1 + V_2 = v(x,t) - v(x+\delta x,t) = -\frac{\partial v}{\partial x} \cdot \delta x \tag{A.6}$$

The introduction of $C_0 = \frac{C}{\delta x}$ as capacitance per unit length and $L_0 = \frac{L_1+L_2}{\delta x}$ as total inductance per unit length lead to the transmission line equations:

$$C_0 \frac{\partial v}{\partial t} = -\frac{\partial i}{\partial x} \qquad L_0 \frac{\partial i}{\partial t} = -\frac{\partial v}{\partial x} \tag{A.7}$$

The combination of these two equations is also known as the telegrapher's equations, a coupled, linear differential system.
The general solutions for the voltage and the current are given as

$$v(x,t) = f(t - \frac{x}{u}) + g(t + \frac{x}{u}) \tag{A.8}$$

$$i(x,t) = \frac{f(t - \frac{x}{u}) - g(t + \frac{x}{u})}{Z_0} \tag{A.9}$$

with the group velocity $u = \sqrt{\frac{1}{L_0 C_0}}$ and the wave impedance $Z_0 = \sqrt{\frac{L_0}{C_0}}$. The functions f and g can be arbitrary differentiable functions as long as an infinite transmission line is assumed.

Reflections If only a transmission line of length l, terminated with a resistive load R_L, is taken into account the two functions f and g have to fullfill Ohm's law:

$$v(l,t) = i(l,t) \cdot R_L \tag{A.10}$$

Insertion of the general solutions for $v(x,t)$ and $i(x,t)$ determines the relation between f and g.

$$f_l(t) + g_l(t) = \frac{R_L}{Z_0}(f_l(t) - g_l(t)) \tag{A.11}$$

$$\Rightarrow \; g_l(t) = \underbrace{\frac{R_L - Z_0}{R_L + Z_0}}_{\text{reflection coeff. } \rho_L} \cdot f_l(t) \tag{A.12}$$

So an incoming signal $f(t)$ is partly reflected at the resistive load, with the ratio ρ_L. For a match of the resistive load R_L and the wave impedance Z_0 no reflections occur, the transmission line is correctly terminated.
As long as the length l of the transmission line is much shorter than the wavelength λ of the signal of interest $l \ll \lambda_{\text{signal}} = \frac{u}{f_{\text{signal}}}$, the voltages and currents present at the two ends of the transmission line are nearly identical and no reflection effect occurs. For short lines and especially high frequencies, the determination of the wave impedance and the correct termination define the quality of the signal transfer.
The typical wave impedance for differential lines is $Z_0 = 100\,\Omega$, with a group velocity of about $u \approx 15\,\text{cm/ns}$.

A.2 Attenuation

The input of the DFAB is designed for measurements with one of three selectable gain stages. Therefore, the signal is split up and attenuated by several resistive voltage dividers. To avoid reflections due to a varying termination (see appendix A.1), the attenuators have to build an effective 50 Ω termination to match the wave impedance of the LEMO input cables. Figure A.2 depicts a single attenuator setup.

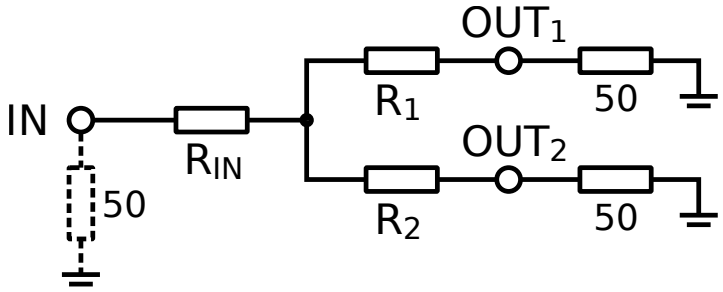


Figure A.2: Schematic setup of an attenuator. An input signal is split into two branches with relative gain stages defined by the resistors R_1 and R_2. The listed values are in Ω.

The setup is determined by three conditional equations:

$$\text{I}: R_{IN} + \left(\frac{1}{R_1 + 50\,\Omega} + \frac{1}{R_2 + 50\,\Omega}\right)^{-1} = 50\,\Omega \tag{A.13}$$

$$\text{II}: R_1 + \left(\frac{1}{R_{IN} + 50\,\Omega} + \frac{1}{R_2 + 50\,\Omega}\right)^{-1} = 50\,\Omega \tag{A.14}$$

$$\text{III}: \frac{50\,\Omega}{R_1 + 50\,\Omega} = g \cdot \frac{50\,\Omega}{R_2 + 50\,\Omega} \tag{A.15}$$

Equations I and II describe an effective resistance of 50 Ω for signals entering the attenuator from IN and OUT1. This condition results in directly in identical values for R_{IN} and R_1. Equation III couples the two gain stages to generate the desired relative ratio g of the outputs OUT1 and OUT2.
The solution of this equation systems leads to

$$R_{IN} = \frac{g+1}{2g+1} \cdot 100\,\Omega - 50\,\Omega \tag{A.16}$$

$$R_1 = R_{IN} \tag{A.17}$$

$$R_2 = \frac{g^2+g}{2g+1} \cdot 100\,\Omega - 50\,\Omega. \tag{A.18}$$

For a relative ratio of $g = 4$ the optimum resistor values are therefore $R_{IN} = R_1 = 5.\bar{5}\,\Omega$ and $R_2 = 172.\bar{2}\,\Omega$. On the DFAB, the next values from the E24 series ($R_1 = 5.6\,|$omega and $R_2 = 180\,\Omega$) are used. In addition, the 50 Ω termination at OUT2 in figure A.2 is replaced by a second, identical attenuator. Thus, the three available gain stages differ by a factor of 5 and 20, respectively.

Appendix B

Schematics

B.1 Connections between FPGA and DFAB

SAMTEC pin name	DFAB signal
IN_1_P	A0 of MUX509 channels 1+2
IN_1_N	A1 of MUX509 channels 1+2
IN_2_P	DWRITE of DRS4
IN_2_N	DENABLE of DRS4
IN_3_P	A3 of DRS4
IN_3_N	A2 of DRS4
IN_4_P	DTAP of DRS4
IN_4_N	PLLLCK of DRS4
IN_5_P	REFCLK+ of DRS4
IN_5_N	REFCLK- of DRS4
IN_6_P	A0 of DRS4
IN_6_N	A1 of DRS4
IN_7_P	RSRLOAD of DRS4
IN_7_N	SRCLK of DRS4
IN_8_P	SRIN of DRS4
IN_8_N	SROUT of DRS4
IN_9_P	A0 of MUX509 channels 3+4
IN_9_N	A1 of MUX509 channels 3+4
IN_11_P	A0 of MUX509 channels 5+6
IN_11_N	A1 of MUX509 channels 5+6
IN_12_P	A0 of MUX509 channels 7+8
IN_12_N	A1 of MUX509 channels 7+8

Table B.1: Assignment of DFAB signals and connector pins to the FEBEX 3B board

B.2 Prototype Board revision 1.0

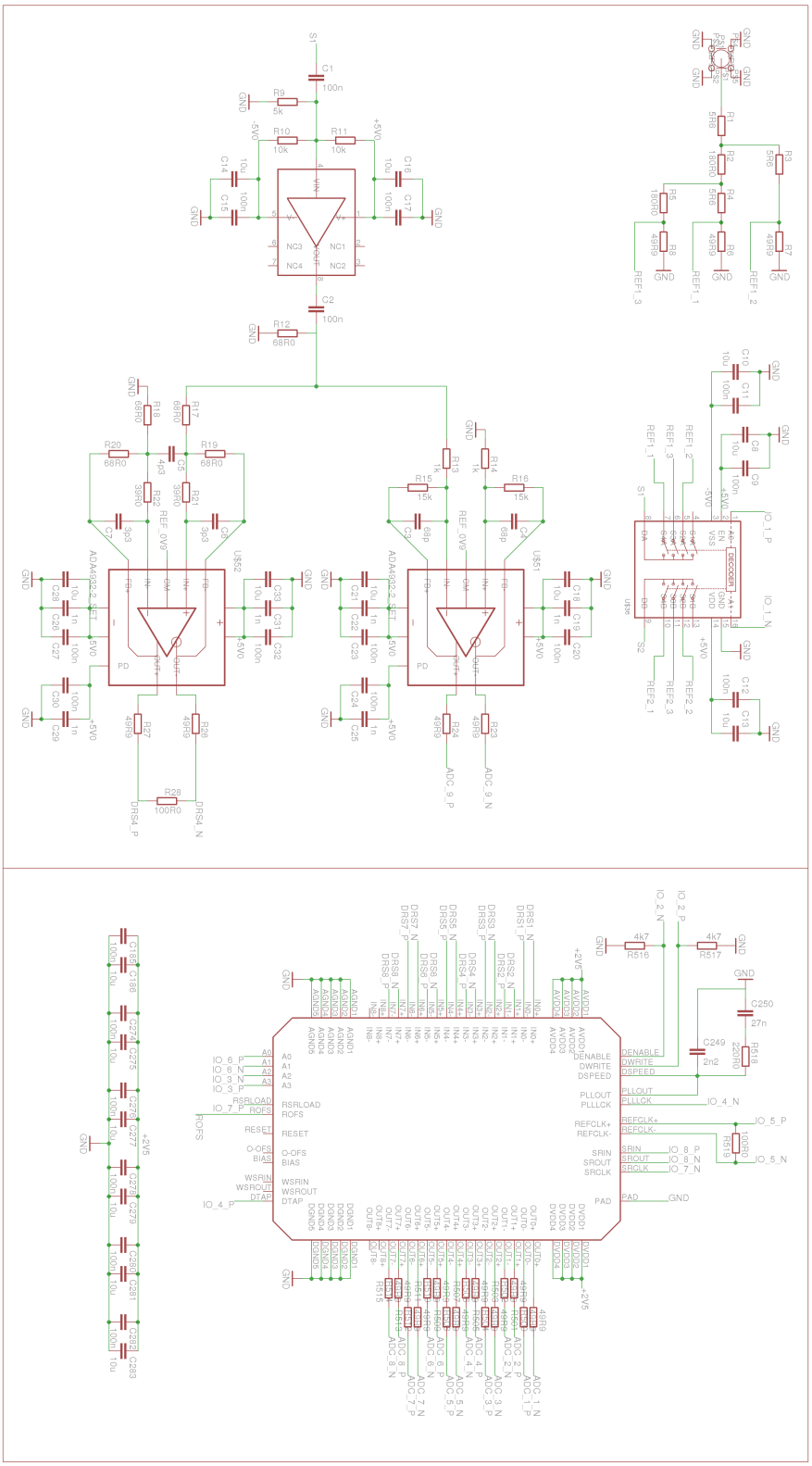


Figure B.1: Schematic of DFAB revision 1.0

B.3 Planned revision 2.0

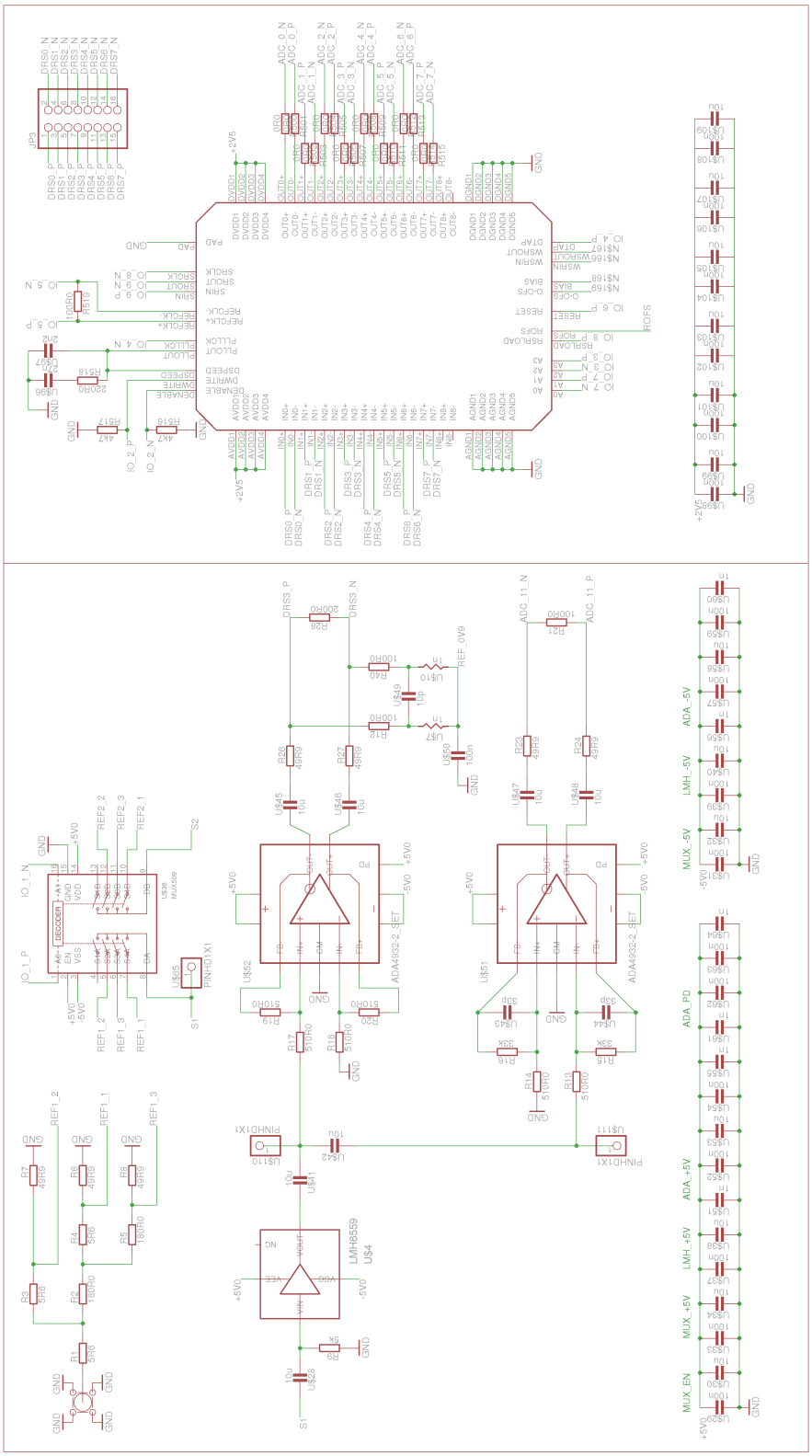


Figure B.2: Schematic of DFAB revision 2.0

Appendix C

Test Firmware

```
library ieee;
use ieee.std_logic_1164.all;

entity drs4_ctrl is
        port
        (
        CLK             : in std_logic; --! 100 MHz clock
        TRIGGER_IN      : in std_logic; --! Trigger input

        SRCLK_OUT       : out std_logic; --! 25 MHz SR clock
        ADCCLK_OUT      : out std_logic; --! 25 MHz ADC clock

        -- Domino Wave Control
        --! Domino Wave enable
        DENABLE_OUT     : out std_logic;
        --! Domino Wave write
        DWRITE_OUT      : out std_logic;

        -- Register configuration
                --! address bits
        A_OUT           : out std_logic_vector ( 3 downto 0 );
        --! shift register
        SRIN_OUT        : out std_logic;

        RSRLOAD_OUT     : out std_logic;

        -- Gain Stage
        GAIN_OUT        : out std_logic_vector ( 7 downto 0 )
    );
end entity drs4_ctrl;

architecture behave of drs4_ctrl is
  signal trigger_int : std_logic;
  signal srclk_int   : std_logic := '0';
  signal adcclk_int  : std_logic := '0';
  signal denable_int : std_logic := '0';
  signal dwrite_int  : std_logic := '0';
  signal a_int       : std_logic_vector ( 3 downto 0 ) := "1010";
  signal srin_int    : std_logic := '0';
  signal rsrload_int : std_logic := '0';

  type type_drs_state is (startup, set_config, set_read, set_write, wait_enable, idle,
      readout_reg, read_cells);
  signal drs_state  : type_drs_state := startup;

begin
  trigger_int <= trigger_in;
  srclk_out   <= srclk_int;
  adcclk_out  <= adcclk_int;
  denable_out <= denable_int;
  dwrite_out  <= dwrite_int;
  a_out       <= a_int;
```

```
srin_out    <= srin_int;
rsrload_out <= rsrload_int;
gain_out    <= "10101010";


PROC_DRS4 : process ( clk )
  variable counter : integer range 0 to 4095 := 0;
  variable clk_counter : integer range 0 to 1 := 0;
  variable flg_register : std_logic := '0';
  variable trigger_last_state : std_logic := '1';
  variable busy : std_logic := '0';
  variable read_end : std_logic := '0';
  variable read_start : std_logic := '0';
  variable toggle_src : std_logic := '0';
  variable flg_trigger : std_logic := '0';
  variable ignore_counter : std_logic := '0';

begin
  if rising_edge ( clk ) then

    -- run ADC clock continuouly
    if clk_counter = 0 then
      adcclk_int <= not adcclk_int;
      clk_counter := clk_counter + 1;
    else
      clk_counter := 0;
    end if;



    -- DRS4 state machine
    case drs_state is

      -- startup process
      when startup =>
        if counter = 2047 then
          drs_state <= set_config;
          counter    := 0;
        elsif counter < 200 then
          if clk_counter = 0 then
            srclk_int <= not srclk_int;
          end if;
            counter := counter + 1;
        else
          counter := counter + 1;
        end if;

      -- set Configuration Register
      when set_config =>
        if flg_register = '0' and counter = 10 and clk_counter = 0 then
          a_int <= "1100";
          flg_register := '1';
          counter := 0;
        elsif flg_register = '0' and counter < 10 then
          counter := counter + 1;
        elsif flg_register = '1' and counter < 16 and clk_counter = 0 then
          srin_int <= '1';
          srclk_int <= not srclk_int;
          counter := counter + 1;
        elsif flg_register = '1' and counter = 16 and clk_counter = 0 then
          flg_register := '0';
          srin_int <= '0';
        elsif flg_register = '0' and counter = 16 then
          a_int <= "1010";
          drs_state <= set_read;
          counter := 0;
        end if;

      -- set Read Shift Register
      when set_read =>
        if flg_register = '0' and counter = 10 and clk_counter = 0 then
```

```
      a_int <= "1011";
      flg_register := '1';
      counter := 0;
    elsif flg_register = '0' and counter < 10 then
      counter := counter + 1;
    elsif flg_register = '1' and counter < 2046 and clk_counter = 0 then
      srclk_int <= not srclk_int;
      counter := counter + 1;
    elsif flg_register = '1' and counter = 2046 and clk_counter = 0 then
      srin_int <= '1';
      srclk_int <= not srclk_int;
      counter := counter + 1;
    elsif flg_register = '1' and counter = 2047 and clk_counter = 0 then
                  srclk_int <= not srclk_int;
      counter := counter + 1;
    elsif flg_register = '1' and counter = 2048 and clk_counter = 0 then
      srin_int <= '0';
      flg_register := '0';
    elsif flg_register = '0' and counter = 2048 then
      a_int <= "1010";
      drs_state <= set_write;
      counter := 0;
    end if;

  -- set Write Shift Register
  when set_write =>
    if flg_register = '0' and counter = 10 and clk_counter = 0 then
      a_int <= "1101";
      flg_register := '1';
      counter := 0;
    elsif flg_register = '0' and counter < 10 then
      counter := counter + 1;
    elsif flg_register = '1' and counter < 16 and clk_counter = 0 then
      srin_int <= '1';
      srclk_int <= not srclk_int;
      counter := counter + 1;
    elsif flg_register = '1' and counter = 16 and clk_counter = 0 then
      flg_register := '0';
      srin_int <= '0';
    elsif flg_register = '0' and counter = 16 then
      a_int <= "1010";
      drs_state <= wait_enable;
      counter := 0;
    end if;

  -- wait for enabling
  when wait_enable =>
    if counter = 100 then
      drs_state <= idle;
      counter := 0;
      denable_int <= '1';
      dwrite_int <= '1';
      flg_register := '0';
    else
      counter := counter + 1;
    end if;

  -- idle mode
  when idle =>
    if trigger_int = '1' and trigger_last_state = '0' then
      dwrite_int <= '0';
      busy := '1';
      flg_trigger := '1';
    elsif flg_trigger = '1' and clk_counter = 0 then
      flg_trigger := '0';
      a_int <= "1011";
      drs_state <= readout_reg;
      counter := 0;
    end if;
    trigger_last_state := trigger_int;
```

```
        -- readout register setup mode
        when readout_reg =>

          if clk_counter = 0 then
            if counter = 0 then
              srin_int <= '0';
              toggle_src := '1';
            elsif counter = 2044 then
              srin_int <= '1';
            elsif counter = 2046 then
              srin_int <= '0';
            elsif counter = 2048 then
              toggle_src := '0';
              a_int <= "1010";
            elsif counter = 2051 then
              a_int <= "1001";
              ignore_counter := '1';
              drs_state <= read_cells;
            end if;

            if counter < 2051 and ignore_counter = '0' then
              counter := counter + 1;
            end if;
            if toggle_src = '1' then
              srclk_int <= not srclk_int;
            end if;
          end if;

        -- readout cells mode
        when read_cells =>
          if clk_counter = 0 then
            if ignore_counter = '1' then
              counter := 0;
              ignore_counter := '0';
            end if;

            if counter = 0 then
              srclk_int <= '1';
              toggle_src := '1';
            elsif counter = 2048 then
              srclk_int <= '0';
              toggle_src := '0';
            elsif counter = 2049 then
              a_int <= "1010";
            elsif counter = 2050 then
              dwrite_int <= '1';
              counter := 0;
              drs_state <= idle;
            end if;

            if toggle_src = '1' then
              srclk_int <= not srclk_int;
            end if;

            if ignore_counter = '0' then
              counter := counter + 1;
            end if;
          end if;

        end case;



    end if;
  end process PROC_DRS4;

end architecture behave;
```

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